






|   |  |  |  |  |
|---|--|--|--|--|
| ZZZ1  | ZZZ2   | ZZZ3   | ZZZ4   | ZZZ5   |
|  |  |  |  |  |
| PCB<br>Part Number = DAZ0UI00101  | PCB<br>Part Number = DA60000V110   | PCB<br>Part Number = DA40001HU10   | PCB<br>Part Number = DA40001HV10   | PCB<br>Part Number = DA60000VU10   |

# Compal Confidential

## VBA10 LA9302P Schematics Document

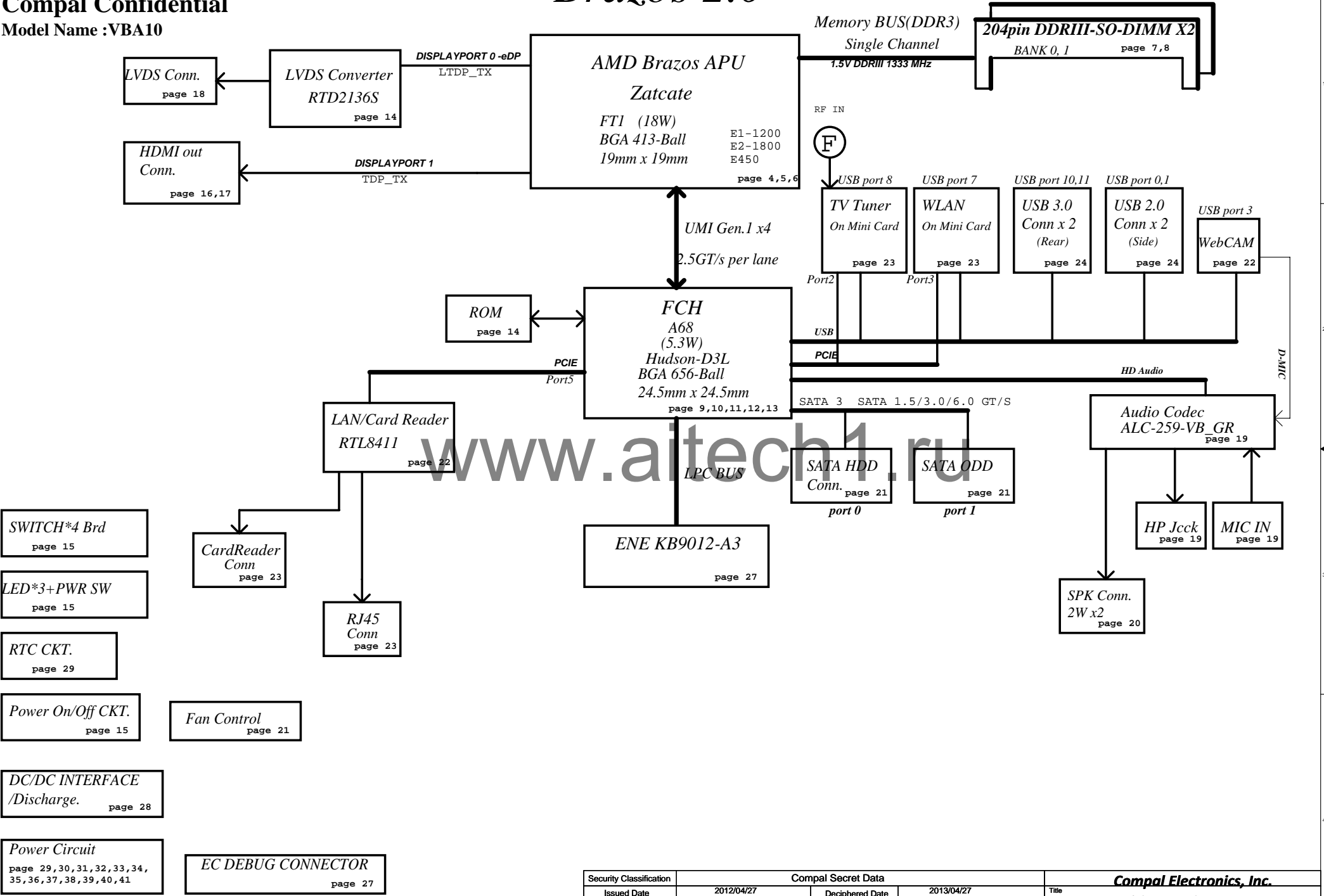
AMD Zatcate APU with DDRIII + FCH Hudson D3L  
AIO M/B

UMA only

REV: 1.0

|   |            |                    |            |                          |                           |
|---|------------|--------------------|------------|--------------------------|---------------------------|
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|   |            |                    |            | Date                     | Tuesday, October 30, 2012 |
|   |            |                    |            | Sheet                    | 1 of 41                   |
|   |            |                    |            | Rev                      | A                         |

# Brazos 2.0



Voltage Rails

| Power Plane  | Description                                   | S1  | S3  | S5  |
|--------------|---|-----|-----|-----|
| VIN          | Adapter power supply (19V)                    | N/A | N/A | N/A |
| B+           | AC or battery power rail for power circuit.   | N/A | N/A | N/A |
| +VSB         | VSB always on power rail                      | ON  | ON  | ON* |
| +3VALW       | 3.3V always on power rail                     | ON  | ON  | ON* |
| +5VALW       | 5V always on power rail                       | ON  | ON  | ON* |
| +1.1VALW     | 1.1V always on power rail                     | ON  | ON  | ON* |
| +APU_CORE    | Core voltage for CPU (0.7-1.2V)               | ON  | OFF | OFF |
| +APU_CORE_NB | 1.0V switched power rail                      | ON  | OFF | OFF |
| +1.5V        | 1.5V power rail for CPU VDDIO and DDRIII      | ON  | ON  | OFF |
| +0.75VS      | 0.75VS switched power rail for DDR terminator | ON  | OFF | OFF |
| +1.05VS      | 1.05V switched power rail for APU VDD10       | ON  | OFF | OFF |
| +1.1VS       | 1.1VS switched power rail                     | ON  | OFF | OFF |
| +1.8VS       | 1.8V switched power rail                      | ON  | OFF | OFF |
| +3VS         | 3.3V switched power rail                      | ON  | OFF | OFF |
| +5VS         | 5V switched power rail                        | ON  | OFF | OFF |
| +3V_LAN      | 3.3V power rail for LAN                       | ON  | ON  | ON  |
| +RTCVCC      | RTC power                                     | ON  | ON  | ON  |

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

| STATE                | SIGNAL | SLP_S1# | SLP_S3# | SLP_S4# | SLP_S5# | +VALW | +V  | +VS |
|----------------------|--------|---------|---------|---------|---------|-------|-----|-----|
| Full ON              | HIGH   | HIGH    | HIGH    | HIGH    | HIGH    | ON    | ON  | ON  |
| S1(Power On Suspend) | LOW    | HIGH    | HIGH    | HIGH    | HIGH    | ON    | ON  | ON  |
| S3(Suspend to RAM)   | LOW    | LOW     | HIGH    | HIGH    | HIGH    | ON    | ON  | OFF |
| S4(Suspend to Disk)  | LOW    | LOW     | LOW     | HIGH    | HIGH    | ON    | OFF | OFF |
| S5(Soft OFF)         | LOW    | LOW     | LOW     | LOW     | LOW     | ON    | OFF | OFF |

| EC SM Bus1 address (EC_SMB1)       |             |     | EC SM Bus2 address (EC_SMB2) |             |     |
|------------------------------------|-------------|-----|------------------------------|-------------|-----|
| Device                             | Address     | HEX | Device                       | Address     | HEX |
| LVDS TR (RTD-2136S)                | 1010-1000xb | A8  | APU                          | 0000-1000xb | 08  |
|                                    |             |     |                              |             |     |
| FCH SM Bus Controller 0 (FCH_SMB0) |             |     | FCH SM Bus Controller 1      |             |     |
| Device                             | Address     | HEX | Device                       | Address     | HEX |
| DDR DIMM1 (FCH_SMB0)               | 1001-0000xb | 90  |                              |             |     |
| DDR DIMM2 (FCH_SMB0)               | 1001-0010xb | 92  |                              |             |     |

Board ID / SKU ID Table for AD channel

| Vcc      | 3.3V +/- 5%  |             |             |             |
|----------|--------------|-------------|-------------|-------------|
| R2676    | 0            |             |             |             |
| Board ID | Rb / Rd / Rf | VAD_BID min | VAD_BID typ | VAD_BID max |
| 0        | 0            | 0 V         | 0 V         | 0 V         |
| 1        | 8.2K +/- 5%  | 0.216 V     | 0.250 V     | 0.289 V     |
| 2        | 18K +/- 5%   | 0.436 V     | 0.503 V     | 0.538 V     |
| 3        | 33K +/- 5%   | 0.712 V     | 0.819 V     | 0.875 V     |
| 4        | 56K +/- 5%   | 1.036 V     | 1.185 V     | 1.264 V     |
| 5        | 100K +/- 5%  | 1.453 V     | 1.650 V     | 1.759 V     |
| 6        | 200K +/- 5%  | 1.935 V     | 2.200 V     | 2.341 V     |
| 7        | NC           | 2.500 V     | 3.300 V     | 3.300 V     |

| PCIE(GPP) Port Table |                     |
|----------------------|---------------------|
| Port                 | Device              |
| 0                    | LAN/Card reader     |
| 1                    | NC                  |
| 2                    | Mini Card(TV Tuner) |
| 3                    | Mini Card(WLAN)     |

| SATA Port Table |                   |
|-----------------|-------------------|
| Port            | Device            |
| 6G              | 0 HDD             |
|                 | 1 ODD             |
|                 | 2 NC              |
|                 | 3 Disabled on D3L |
|                 | 4 Disabled on D3L |
|                 | 5 Disabled on D3L |

| USB Port Table |         |      |                     |
|----------------|---------|------|---------------------|
| USB 2.0        | USB 1.1 | Port | Device              |
| EHCI           | OHCI    | 0    | USB20- (Rear I/O)   |
|                |         | 1    | USB20 (Rear I/O)    |
|                |         | 2    | NC                  |
|                |         | 3    | Web Camera          |
|                |         | 4    | Disabled on D3L     |
| EHCI           | OHCI    | 5    | NC                  |
|                |         | 6    | NC                  |
|                |         | 7    | Mini Card(WLAN)     |
|                |         | 8    | Mini Card(TV Tuner) |
|                |         | 9    | Disabled on D3L     |
| XHCI (USB 3.0) |         | 10   | USB (side I/O)      |
|                |         | 11   | USB (side I/O)      |
|                |         | 12   | Disabled on D3L     |
|                |         | 13   | Disabled on D3L     |

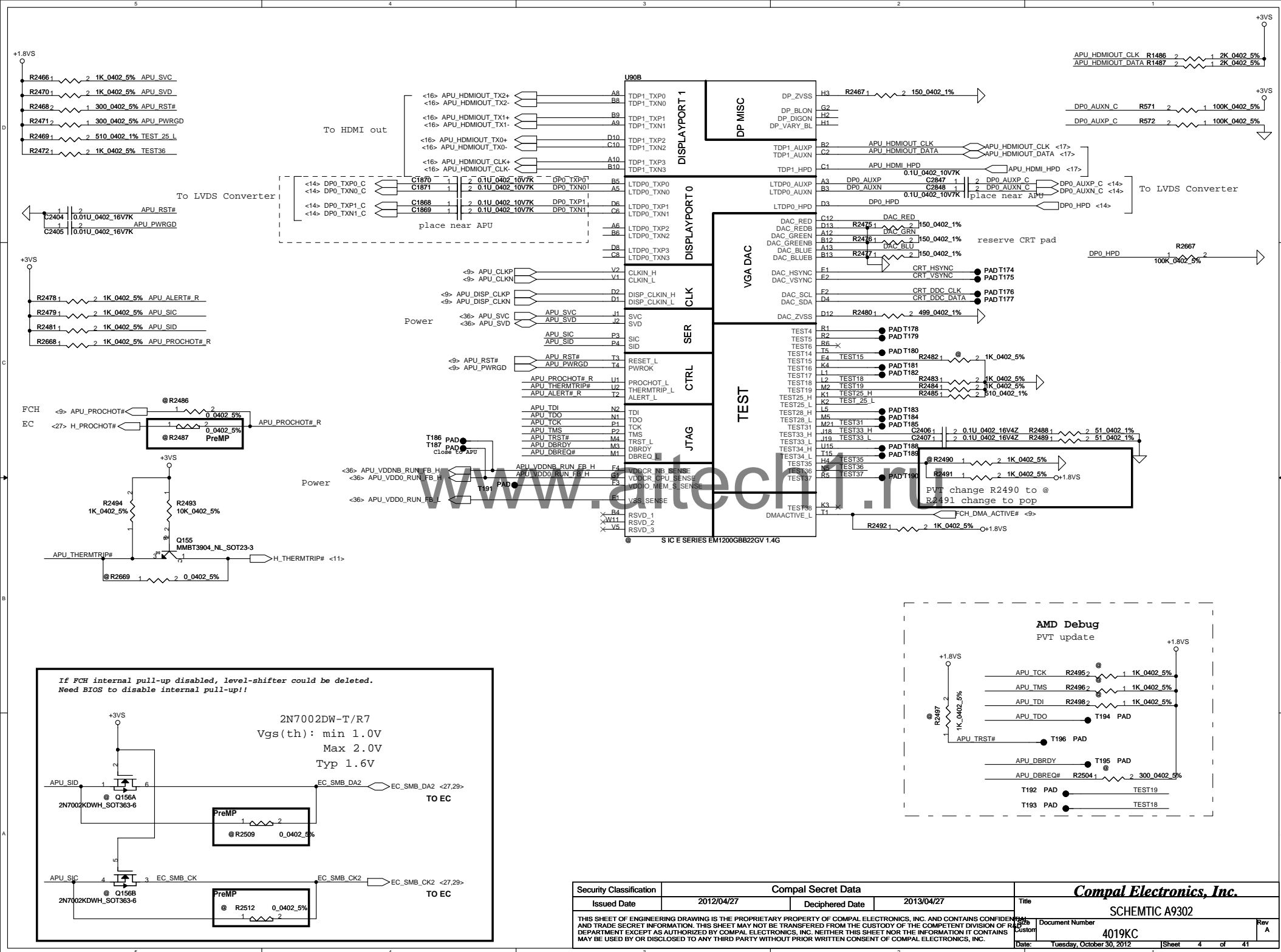
| BTO Item      | BOM Structure |
|---------------|---------------|
| APU (E-450)   | 450@          |
| APU (E1-1200) | 1200@         |
| APU (E2-1800) | 1800@         |
| APU (E- 350D) | 350D@         |
| HUDSON-D3L    | D3L@          |
| ME components | CONN@         |
| Unpop         | @             |
| SKU IO Select | GPIO189_H@    |
|               | GPIO189_L@    |
|               | GPIO190_H@    |
|               | GPIO190_L@    |

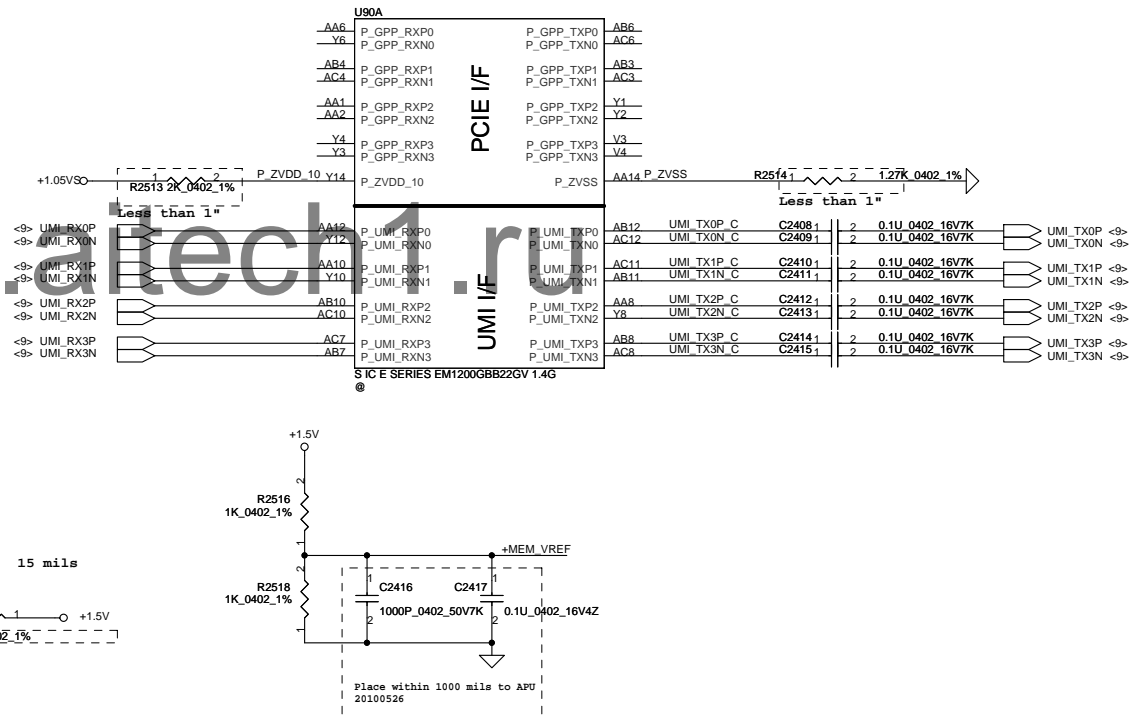
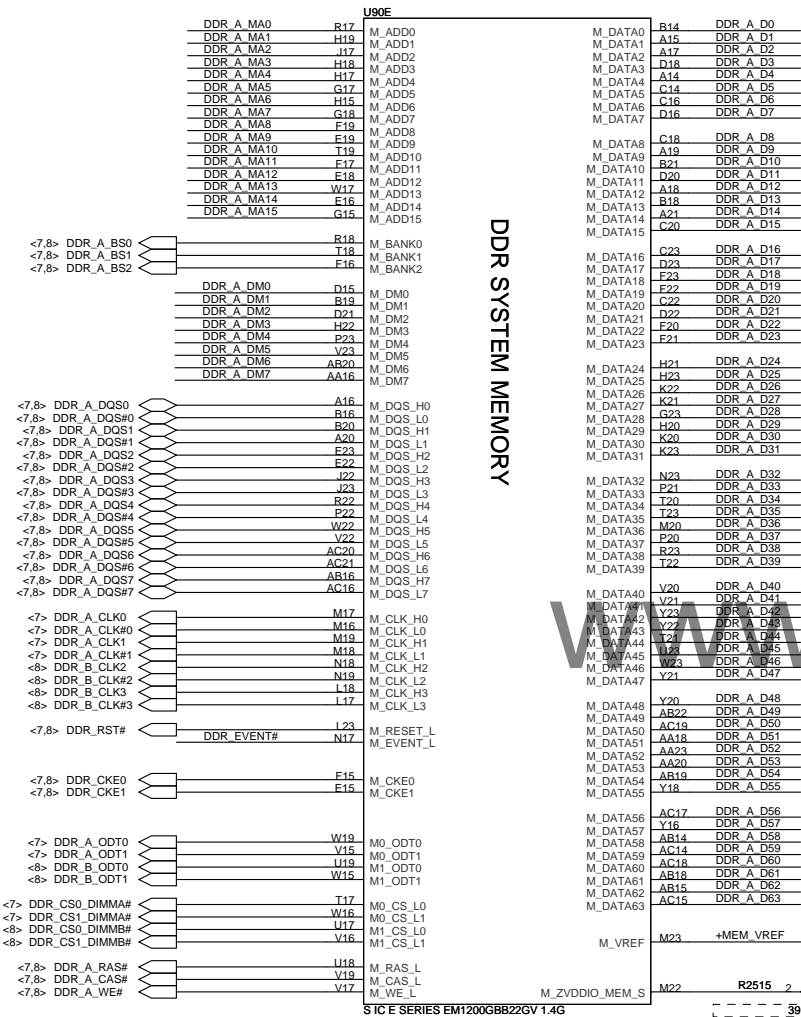
SKU ID(Project) Table

| Project_ID2 (GPIO189) | Project_ID1 (GPIO190) | SKU             |            |
|-----------------------|-----------------------|-----------------|------------|
| 0                     | 0                     | UMA 4319KC38L01 | 1800@ D3L@ |
| 0                     | 1                     | UMA 4319KC38L02 | 1200@ D3L@ |
| 1                     | 0                     | UMA 4319KC38L03 | 450@ D3L@  |
| 1                     | 1                     | UMA 4319KC38L04 | 350D@ D3L@ |

| BOARD ID Table |              |
|----------------|--------------|
| Board ID       | PCB Revision |
| * 0            | 0.1          |
| 1              | 0.2          |
| 2              | 1.0          |
| 3              |              |
| 4              |              |

|   |                    |                 |            |                          |                           |               |
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|   |                    |                 |            | Custom                   | 4019KC                    | A             |
|   |                    |                 |            | Date:                    | Tuesday, October 30, 2012 | Sheet 3 of 41 |





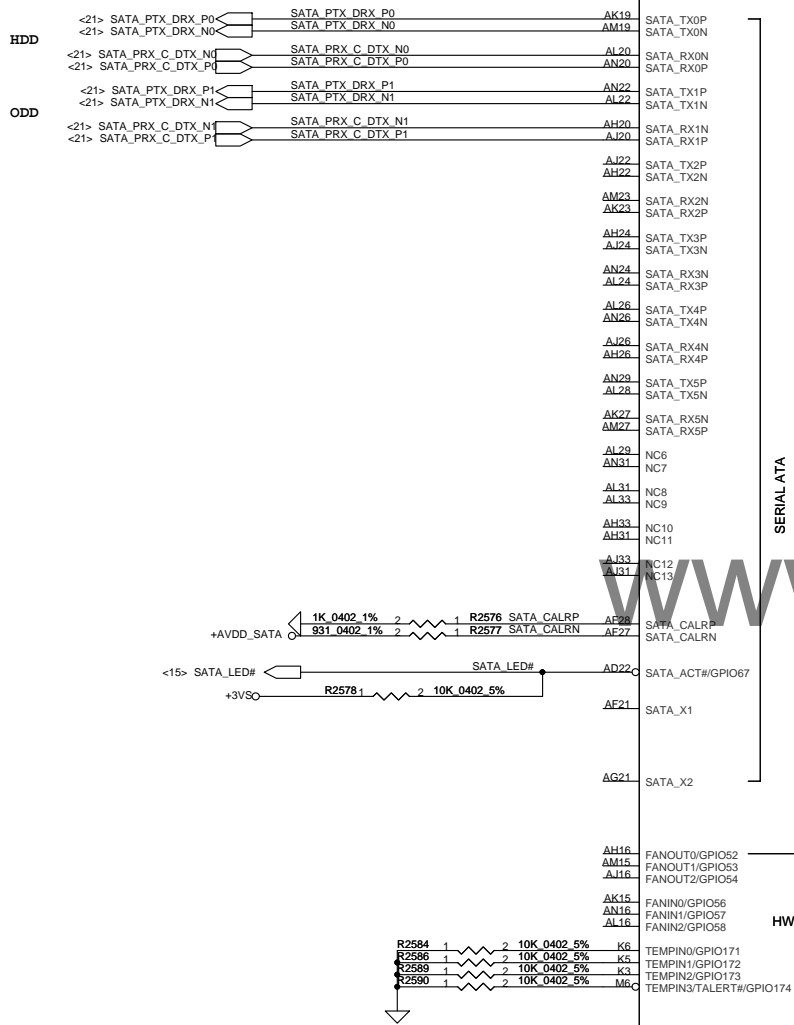




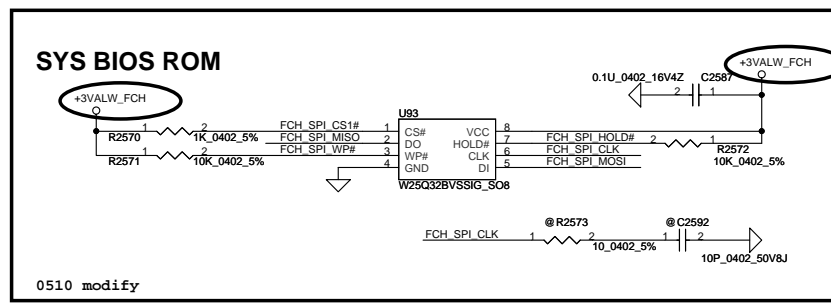








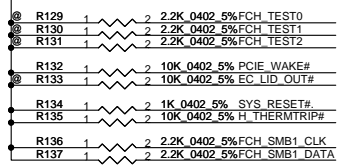
@ 2180755011A14HUDSON\_FCBGA656



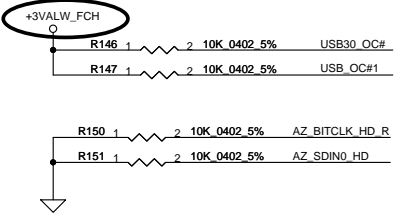
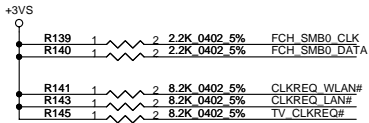
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|   |            |                    |            | Date: Tuesday, October 30, 2012 | Sheet 10 of 41 |

+3VALW\_FCH

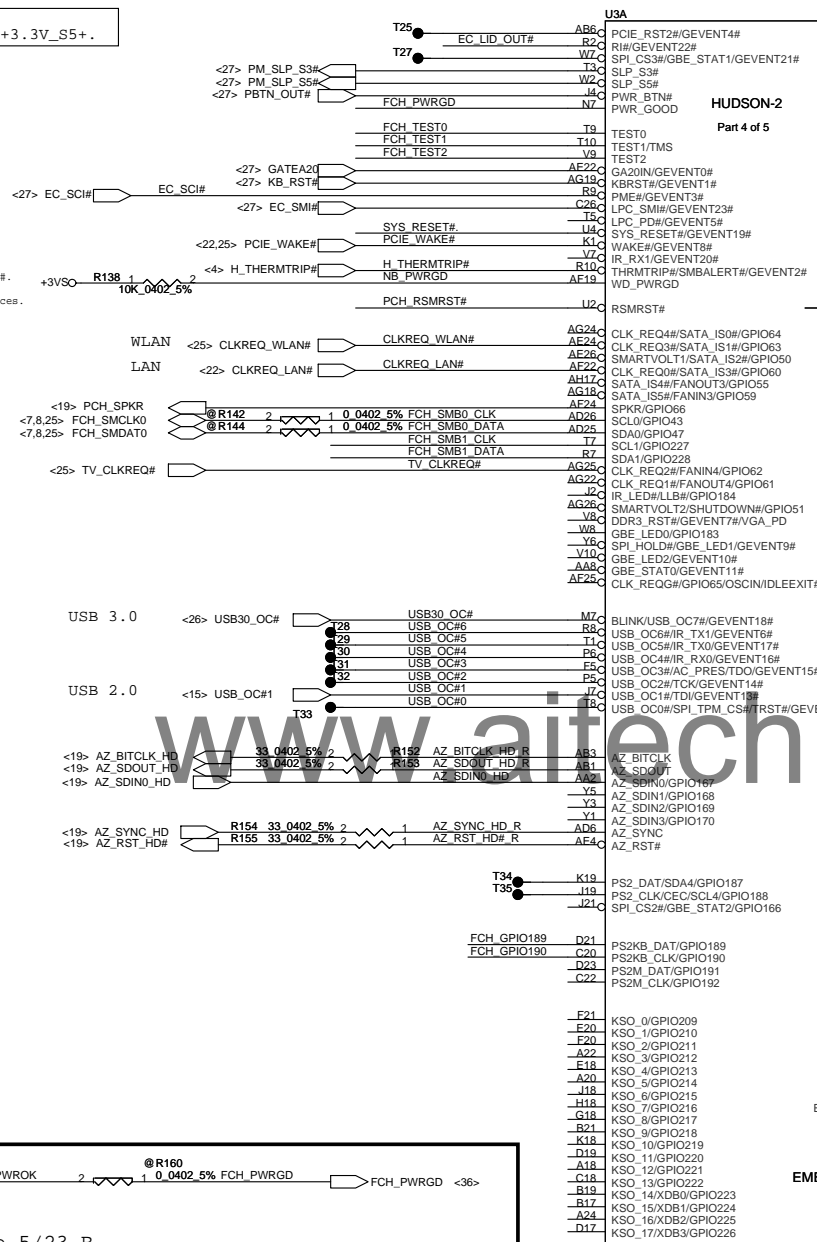
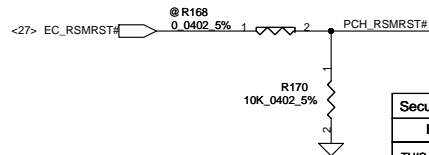
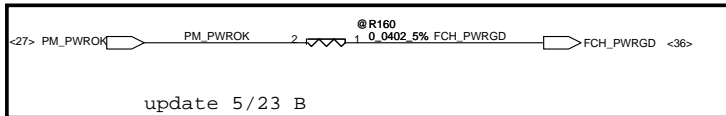
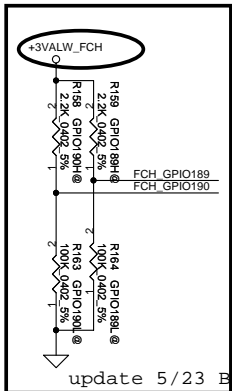
PCH\_PCIE\_WAKE# S5+ mode Implemented:  
Pulled-up with a 10-K? 5% resistor to +3.3V\_S5+.



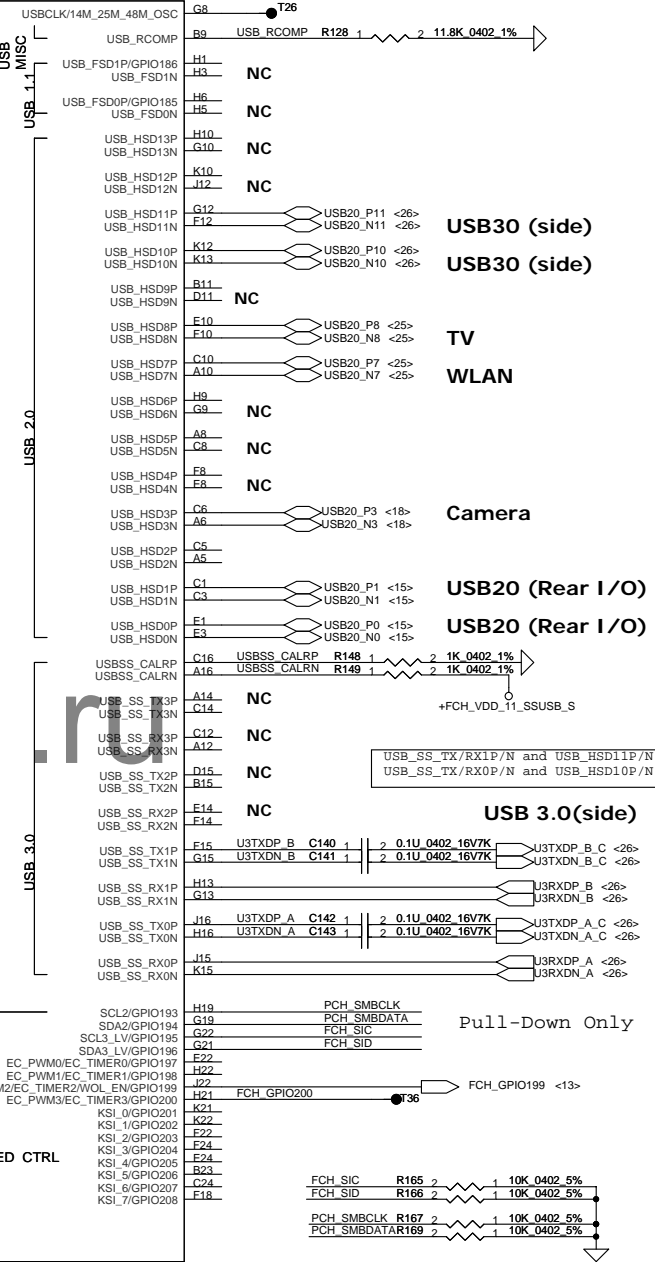
PWR\_GOOD de-assertion does not assert SYS\_RESET#.  
Pulled up to +3.3V\_S0 rail and left unconnected to any other devices.



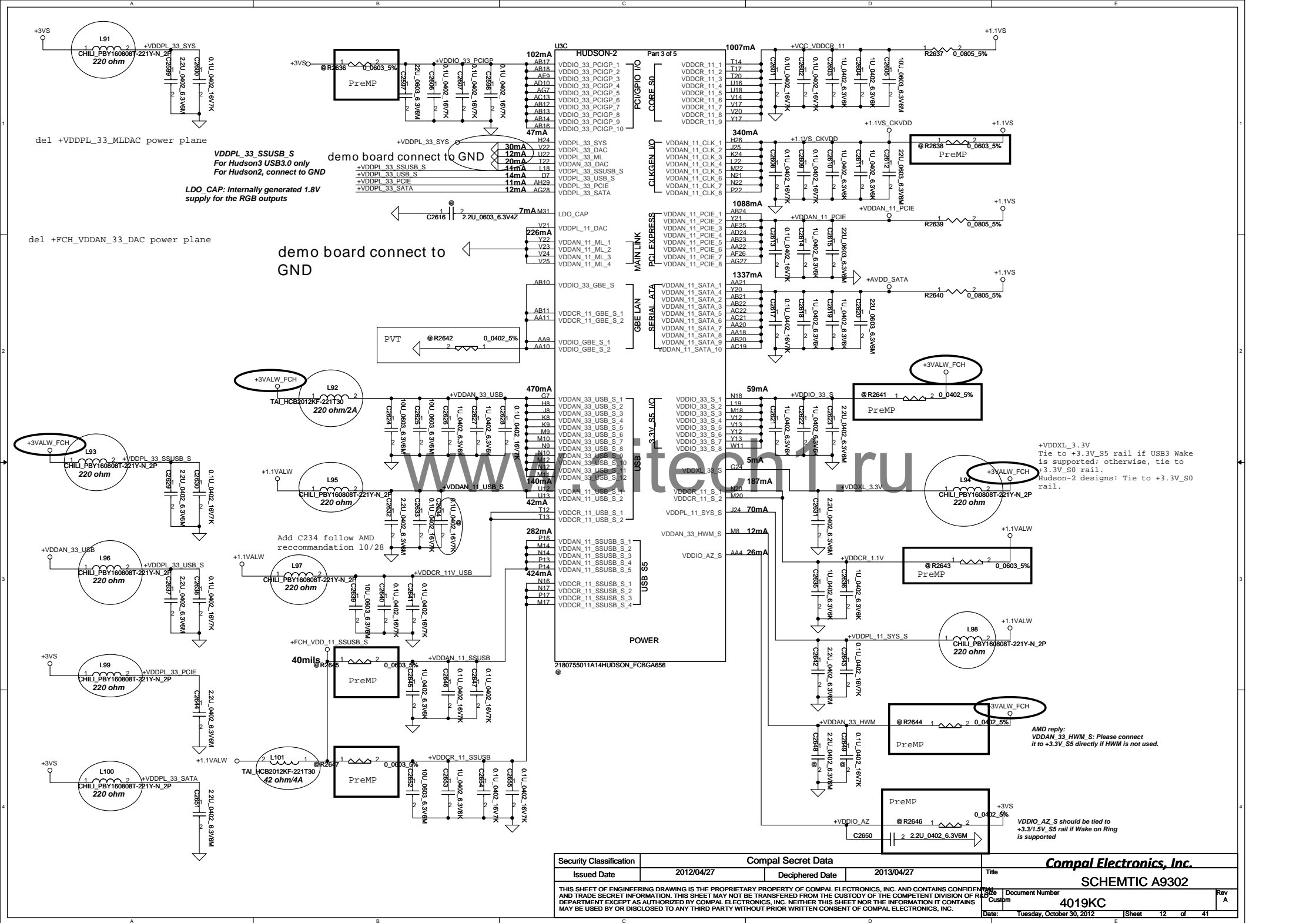
If VDDIO\_AZ\_S power is +1.5V\_S5:  
SDIN0 is not connected to +3.3V device.



2180755011A14HUDSON\_FCBGA656 @



|   |            |                    |            |                          |                           |
|---|------------|--------------------|------------|--------------------------|---------------------------|
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|   |            |                    |            | Date:                    | Tuesday, October 30, 2012 |
|   |            |                    |            | Sheet                    | 11 of 41                  |



# DEBUG STRAPS

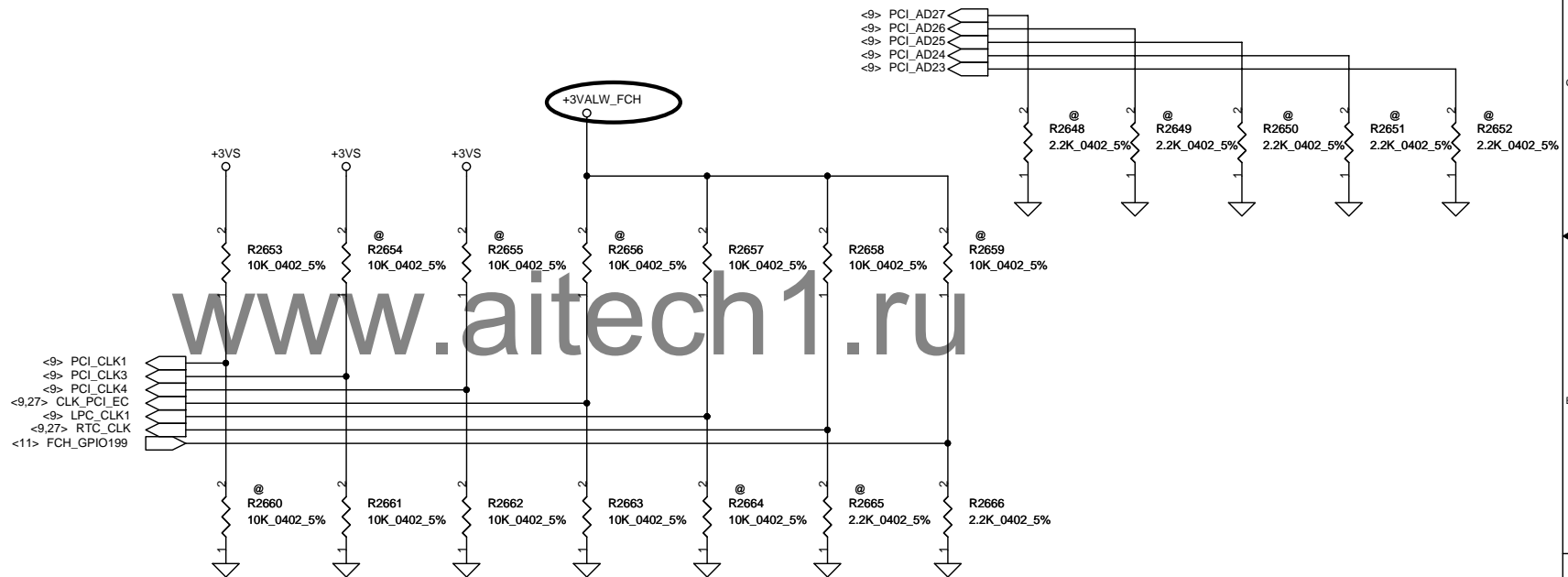
## STRAP PINS

FCH\_GPIO199

FCH HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

|           | PCI_CLK1                   | PCI_CLK3                      | PCI_CLK4                     | LPC_CLK0_EC            | LPC_CLK1                  | EC_PWM2            | RTC_CLK                             |
|-----------|----------------------------|-------------------------------|------------------------------|------------------------|---------------------------|--------------------|-------------------------------------|
| PULL HIGH | ALLOW PCIE GEN2<br>DEFAULT | USE DEBUG STRAPS              | NON FUSION CLOCK MODE        | EC ENABLED             | CLKGEN ENABLED<br>DEFAULT | LPC ROM            | S5 PLUS MODE<br>DISABLED<br>DEFAULT |
| PULL LOW  | FORCE PCIE GEN1            | IGNORE DEBUG STRAP<br>DEFAULT | FUSION CLOCK MODE<br>DEFAULT | EC DISABLED<br>DEFAULT | CLKGEN DISABLE            | SPI ROM<br>DEFAULT | S5 PLUS MODE<br>ENABLED             |

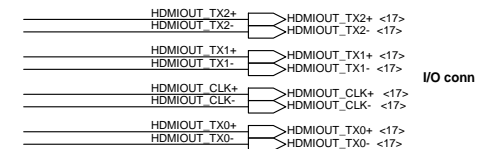
|           | PCI_AD27               | PCI_AD26                          | PCI_AD25                                | PCI_AD24                           | PCI_AD23                        |
|-----------|------------------------|-----------------------------------|---|------------------------------------|---------------------------------|
| PULL HIGH | USE PCI PLL<br>DEFAULT | DISABLE ILA<br>AUTORUN<br>DEFAULT | Normal REFCLK<br>termination<br>DEFAULT | USE DEFAULT PCIE STRAPS<br>DEFAULT | DISABLE PCI MEM BOOT<br>DEFAULT |
| PULL LOW  | BYPASS PCI PLL         | ENABLE ILA<br>AUTORUN             | Inverted REFCLK<br>termination          | USE EEPROM PCIE STRAPS             | ENABLE PCI MEM BOOT             |



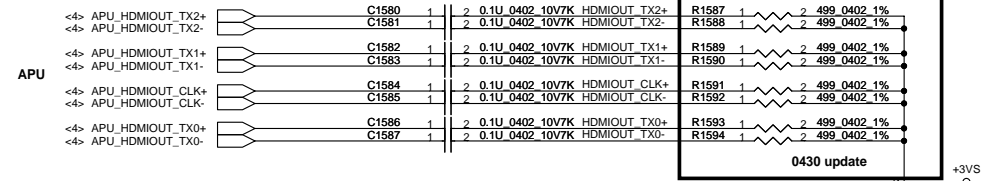
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|   |                    |                 |            | 4019KC                   | A        |
| Date: Tuesday, October 30, 2012   |                    |                 |            | Sheet                    | 13 of 41 |



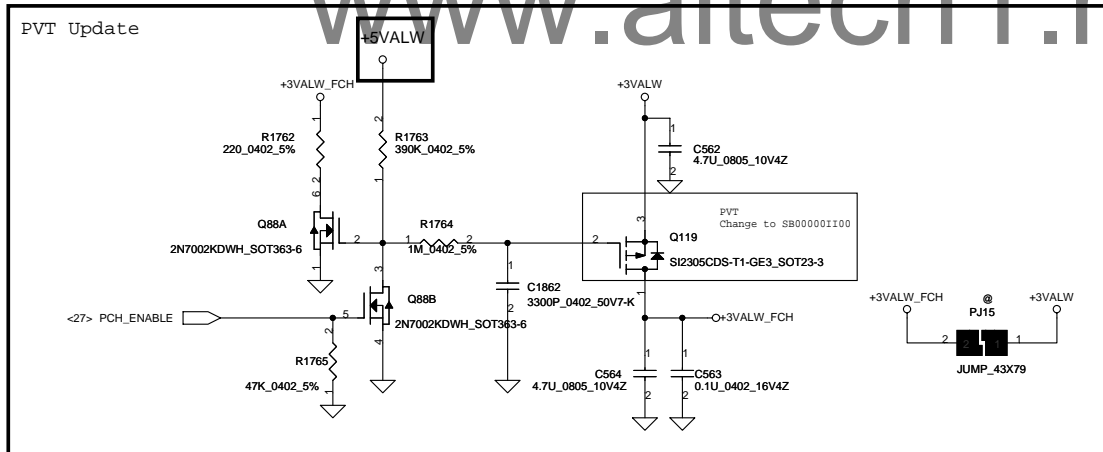
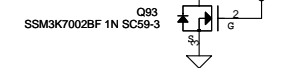




AMD use 499 Ohm for termination



C & R close to JI01 as short as possible



|   |                    |                 |            |                 |                           |                |
|---|--------------------|-----------------|------------|-----------------|---------------------------|----------------|
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|   |                    |                 |            | Date:           | Tuesday, October 30, 2012 | Sheet 16 of 41 |



# HDMI-OUT Level Shift

PU put at APU

<4> APU\_HDMIOUT\_DATA

<4> APU\_HDMIOUT\_CLK

2N7002-KDWH-SOT363-6

Q94A

Q94B

2N7002-KDWH-SOT363-6

+3V5

HDMIOUT\_SDATA

HDMIOUT\_SCLK

Q51

MMBT3904-NL-SOT23-3

R771

100K\_0402\_5%

2PCH\_OUT\_DET

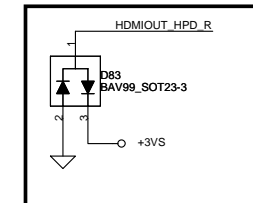
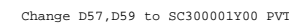
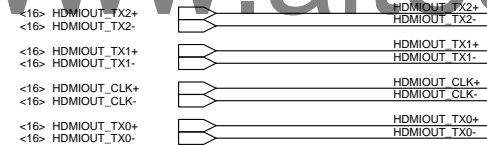
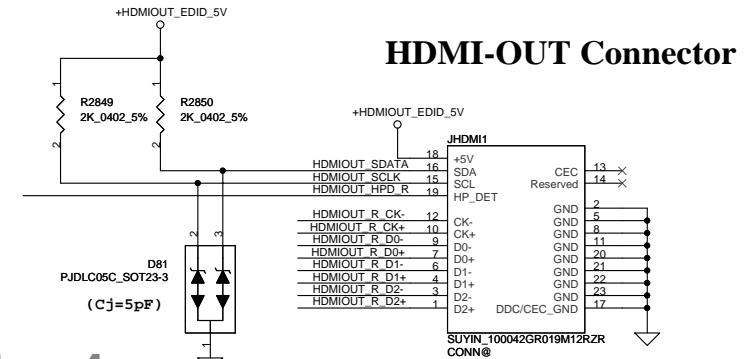
R501

10K\_0402\_5%

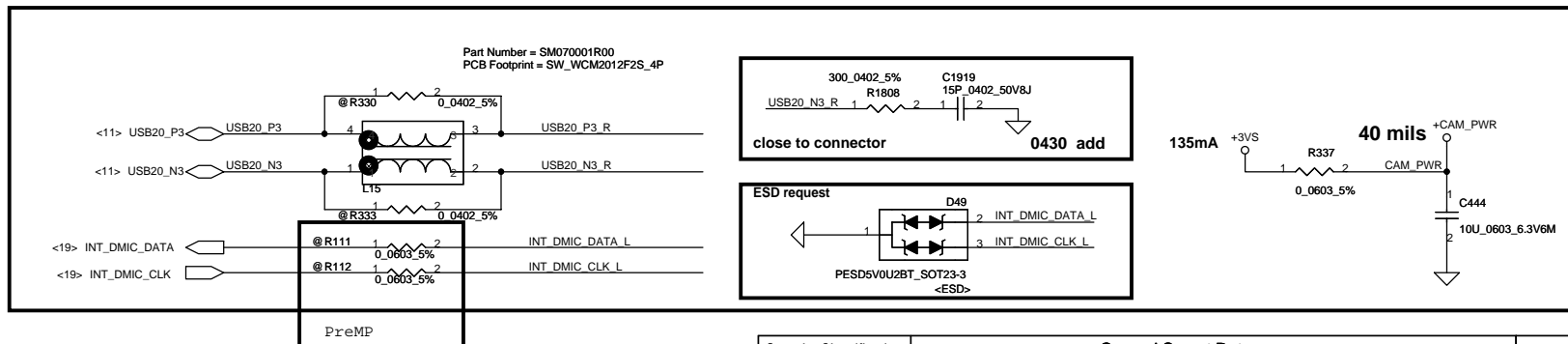
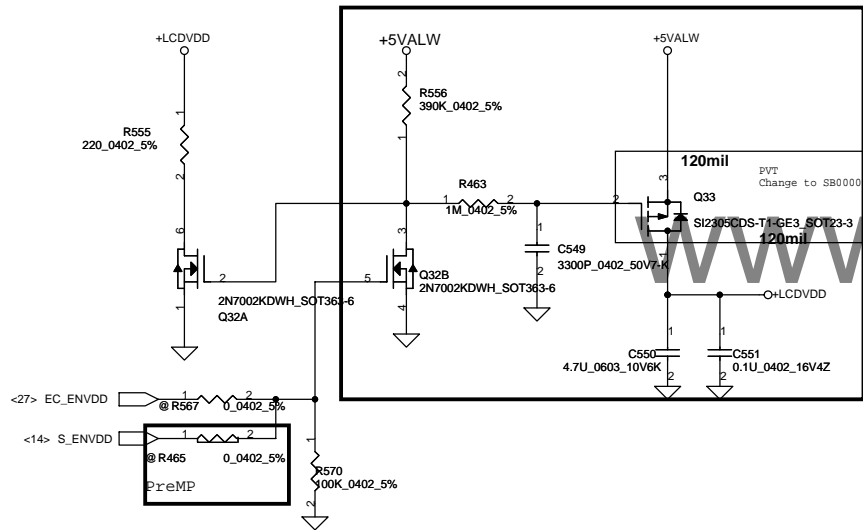
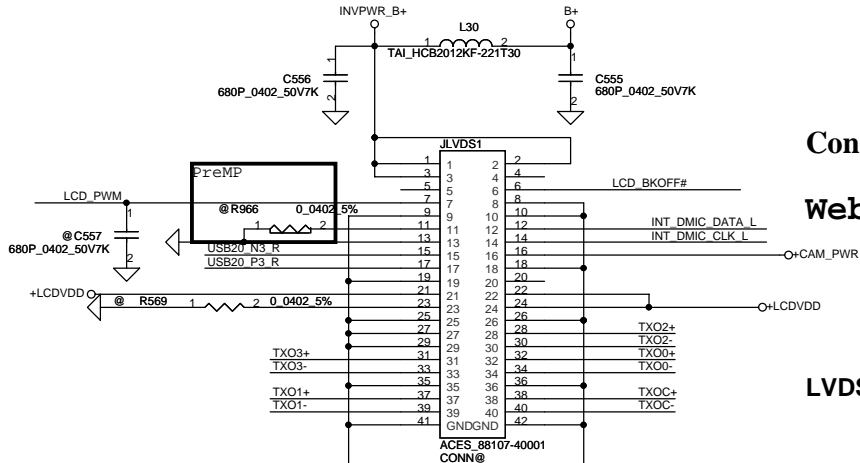
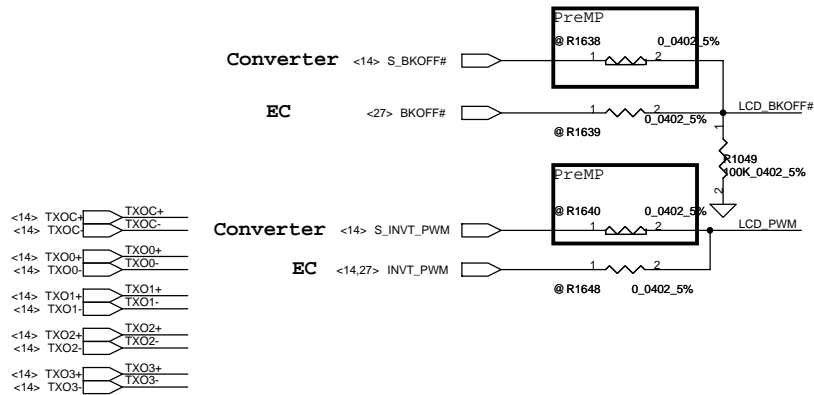
R770

HDMIOUT\_HPD\_R

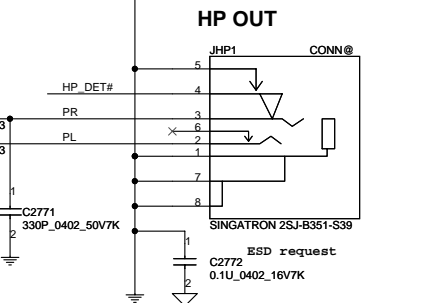
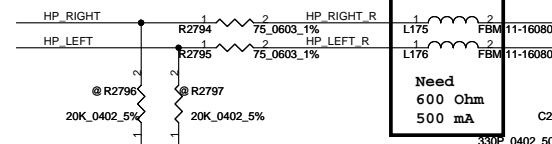
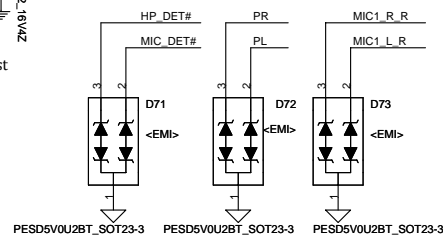
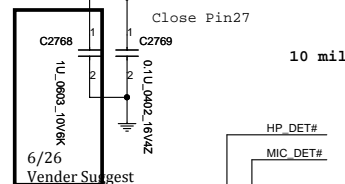
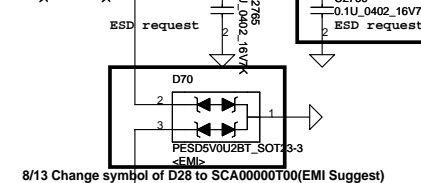
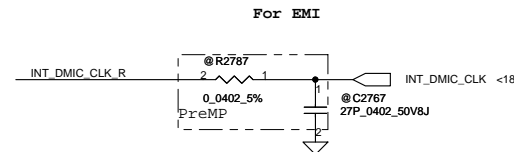
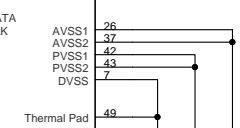
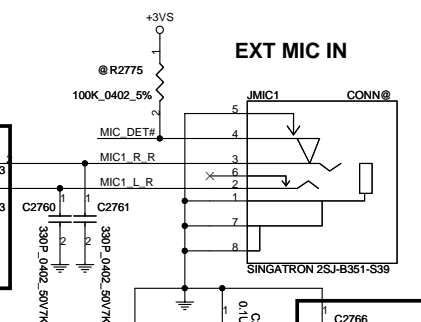
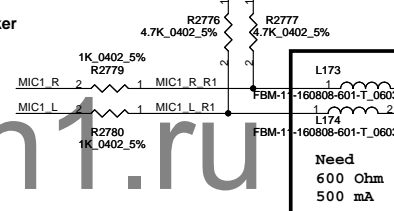
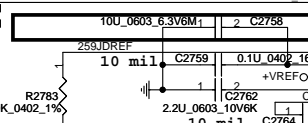
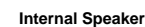
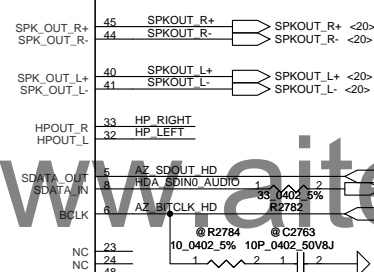
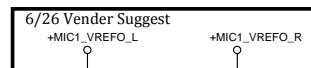
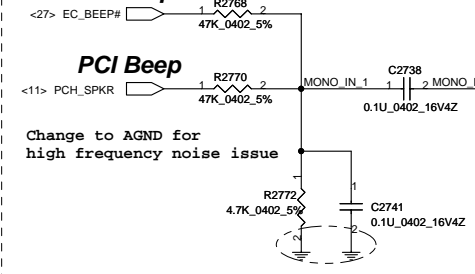
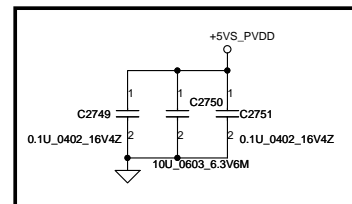
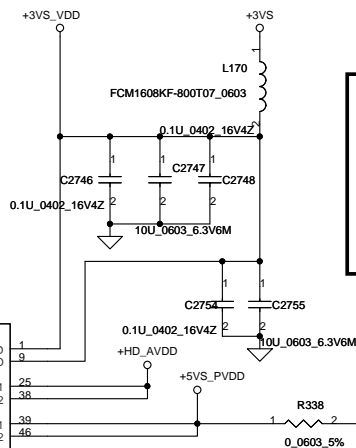
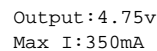
PVT update



|  |            |                    |            |  |                |
|--|------------|--------------------|------------|--|----------------|
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|  |            |                    |            | 4019KC   |                |
|  |            |                    |            | Date: Tuesday, October 30, 2012                          | Sheet 17 of 41 |

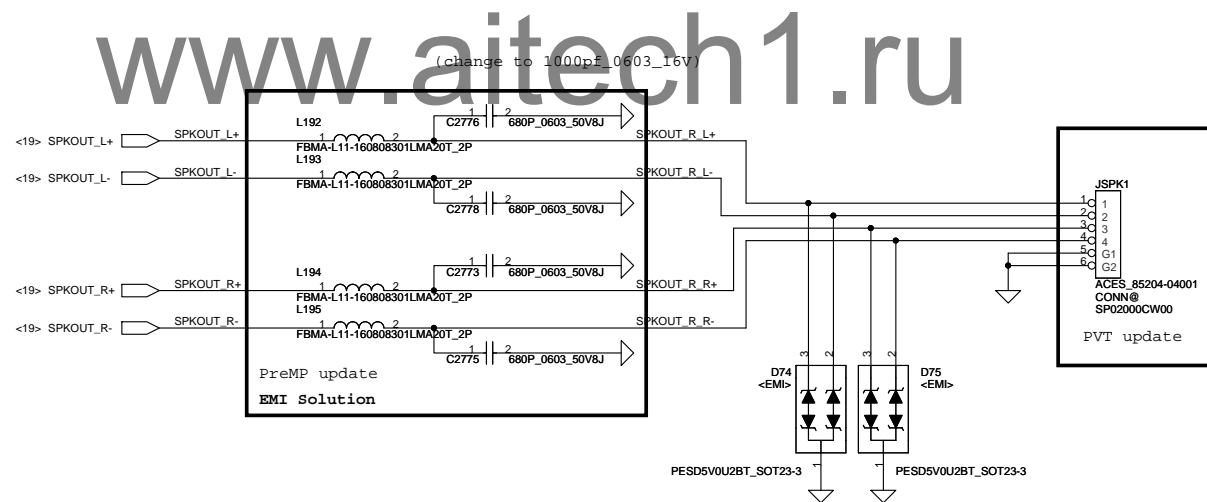


|   |                    |                           |                          |                 |
|---|--------------------|---------------------------|--------------------------|-----------------|
| Security Classification   | Compal Secret Data |                           | Compal Electronics, Inc. |                 |
| Issued Date   | 2012/04/27         | Deciphered Date           | 2013/04/27               | Title           |
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| Document Number   |                    | 4019KC                    |                          | Rev A           |
| Date  |                    | Tuesday, October 30, 2012 |                          | Sheet 18 of 41  |



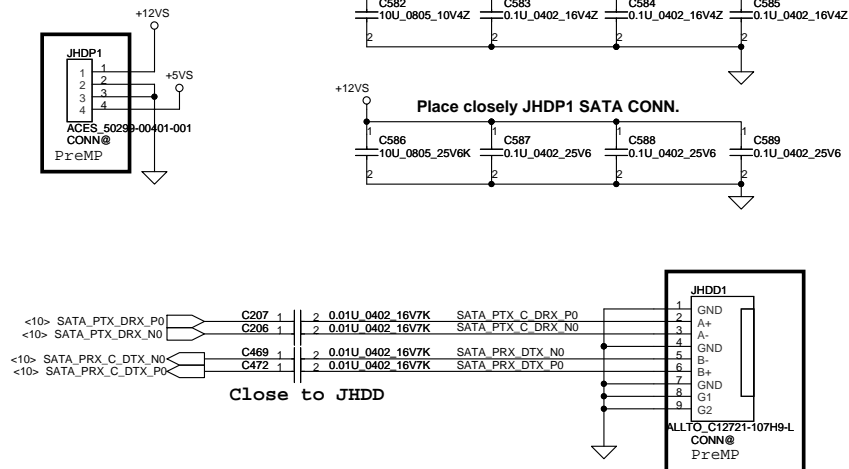
| Sense Pin | Impedance | Codec Signals      |
|-----------|-----------|--------------------|
| SENSE A   | 39.2K     | HP-OUT (PIN 32,33) |
|           | 20K       | MIC1 (PIN 21, 22)  |

|   |                    |                 |            |   |   |  |
|---|--------------------|-----------------|------------|---|---|--|
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| Issued Date   | 2012/04/27         | Deciphered Date | 2013/04/27 | Title   |   |  |
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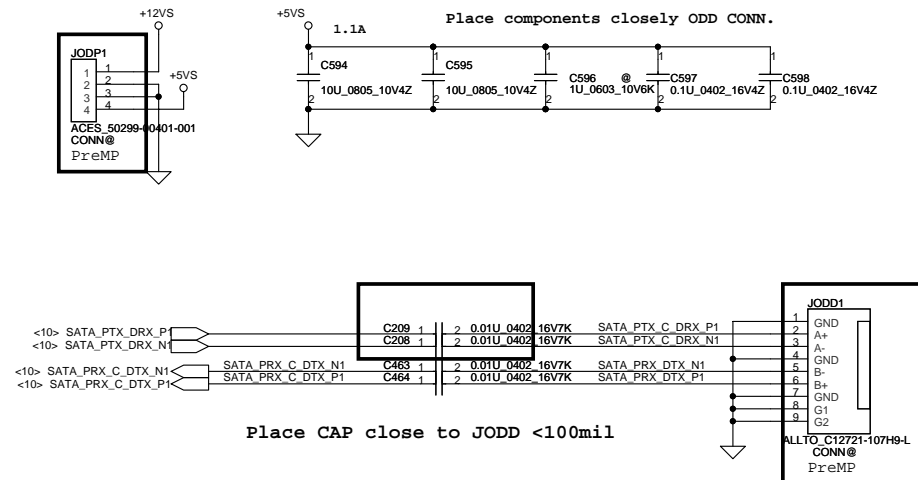


|   |                    |                 |            |                          |                           |
|---|--------------------|-----------------|------------|--------------------------|---------------------------|
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|   |                    |                 |            | Sheet                    | 20 of 41                  |

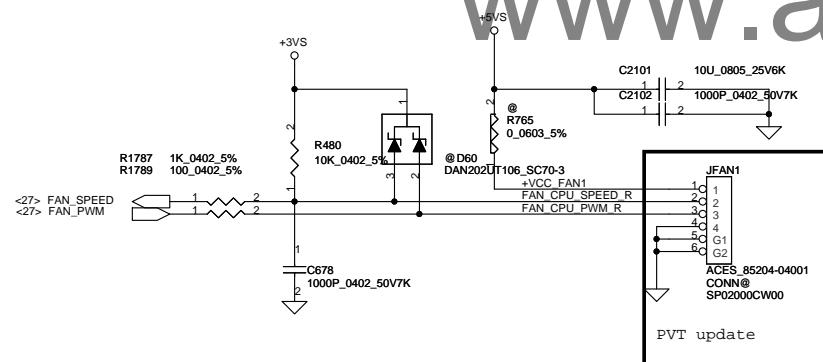
## SATA HDD Conn.



## SATA ODD Conn

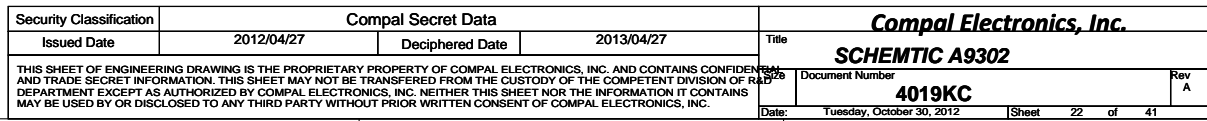
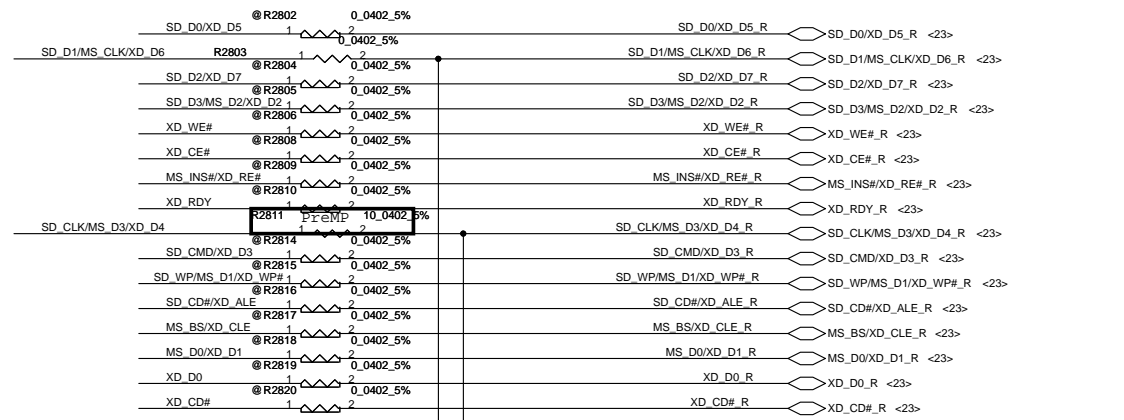


## FAN Control Circuit

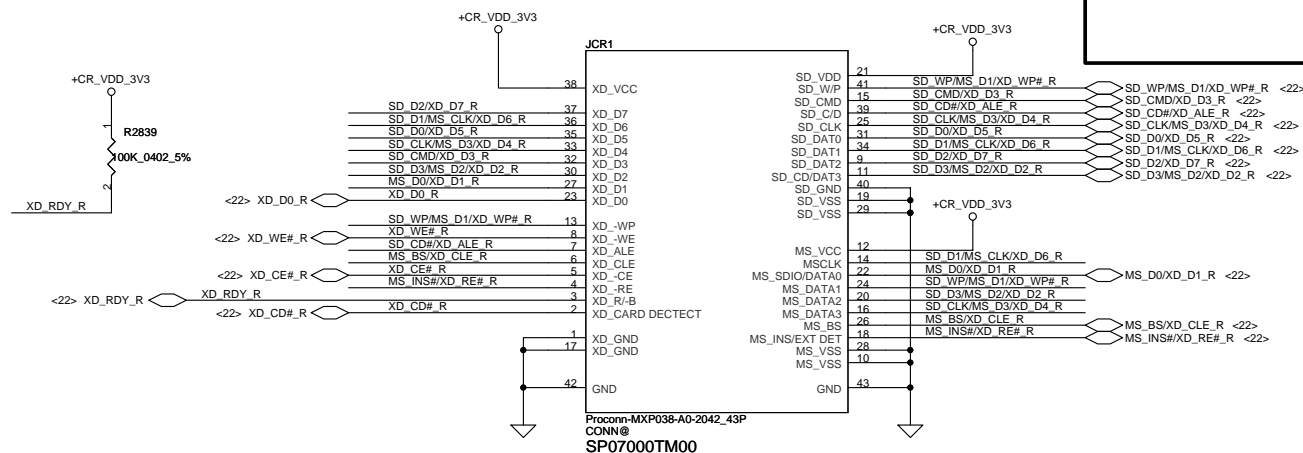
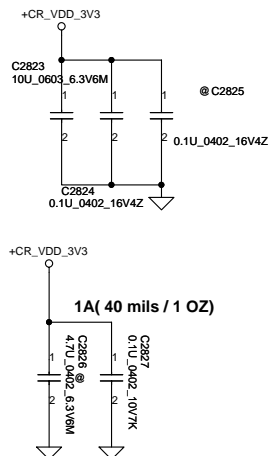
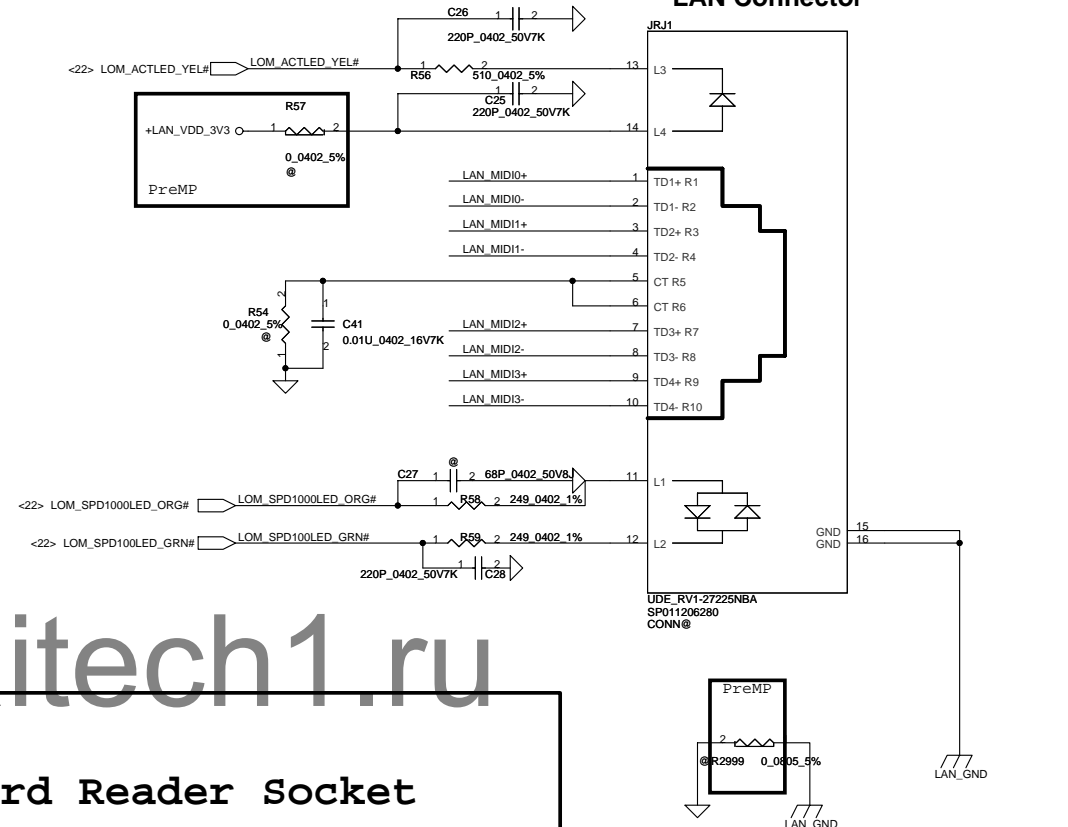
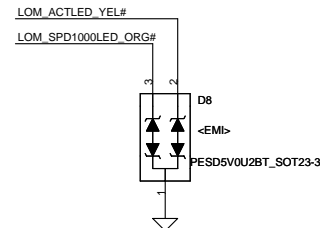
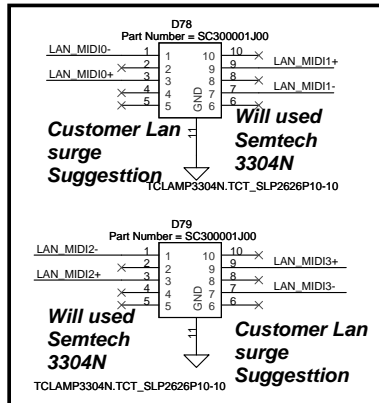
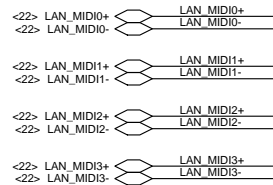


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|   |                    |                 |            |                          |                           |
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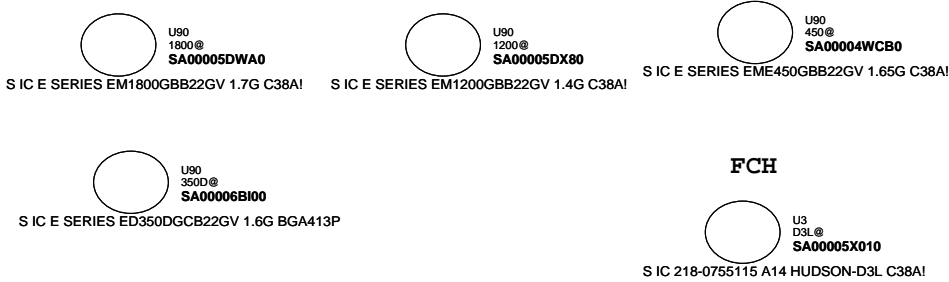


## PVT Combine Transformer to RJ45

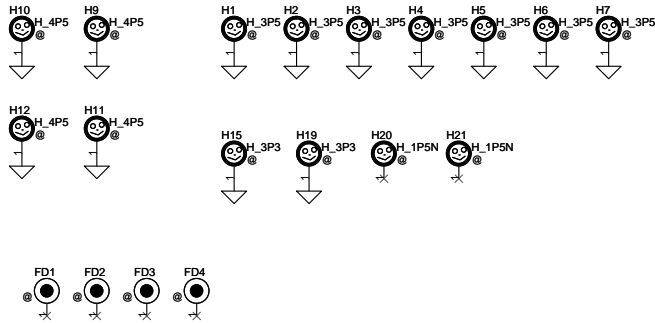


|   |            |                           |            |   |          |
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|   |            |                           |            | Document Number<br><b>4019KC</b>                          | A        |
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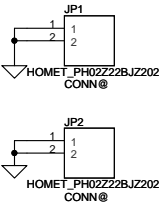
APU



Screw Hole



PCH heat sink

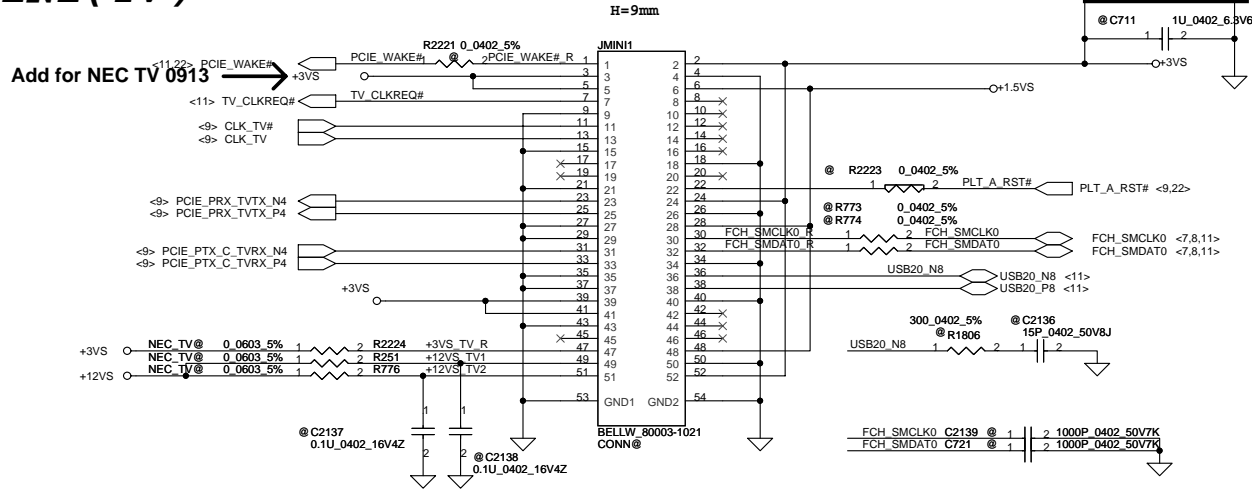


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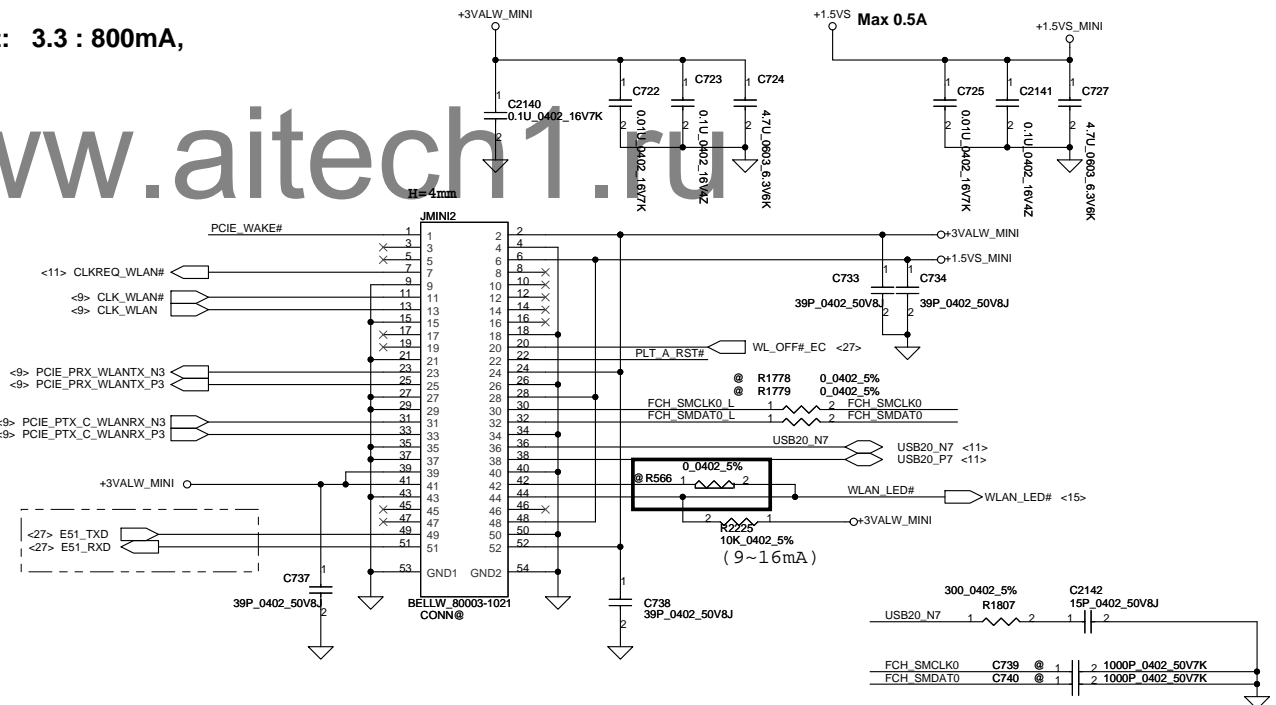
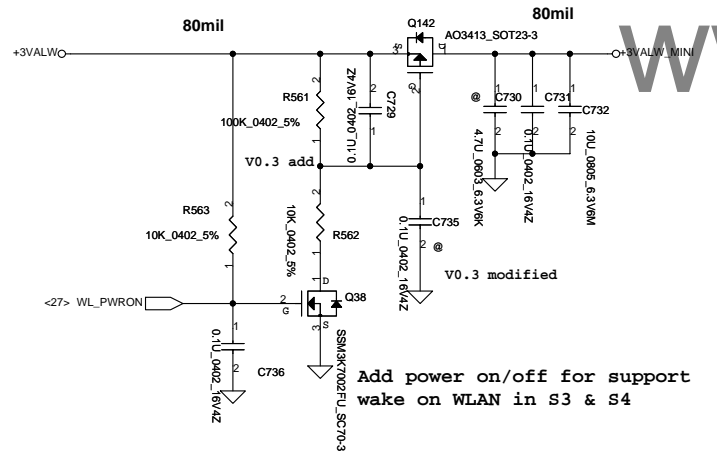
# MINI (TV)

Mini Card Slot 1---TV tuner Current: 3.3 : 2750mA, 1.5: 500mA

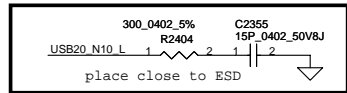


## WLAN

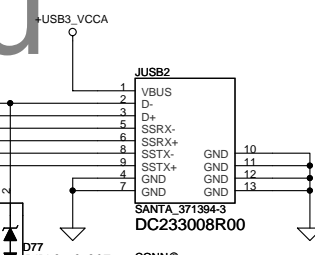
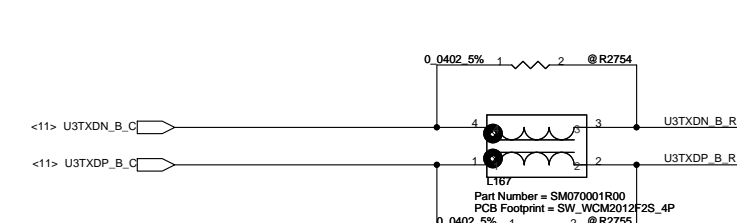
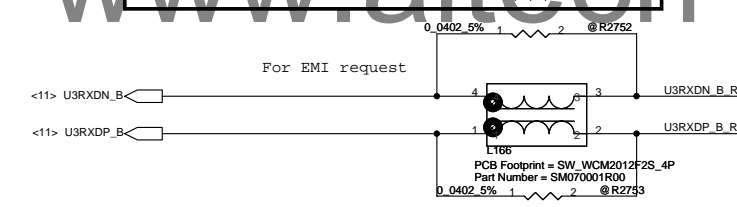
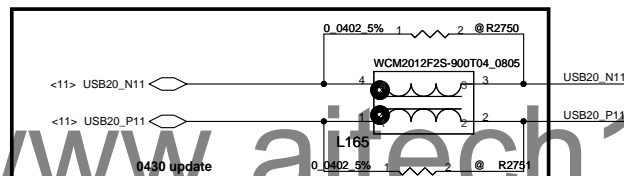
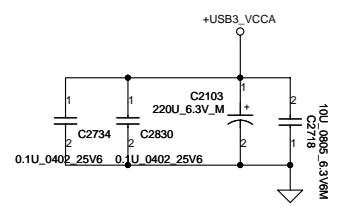
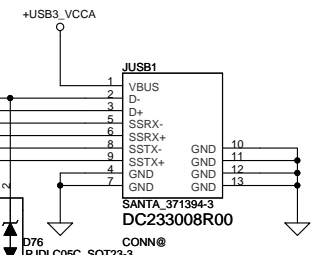
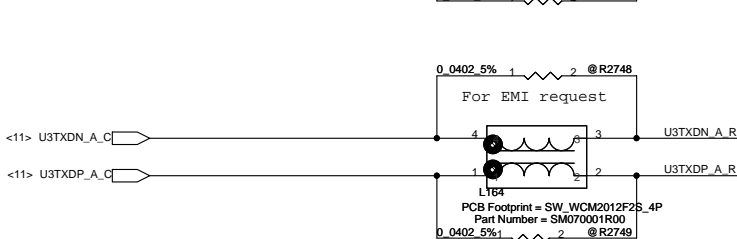
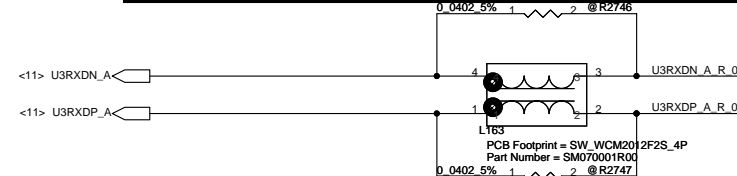
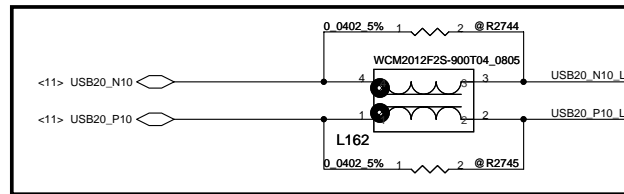
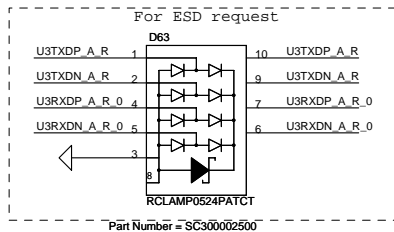
Mini Card Slot 2--- WLAN Current: 3.3 : 800mA,



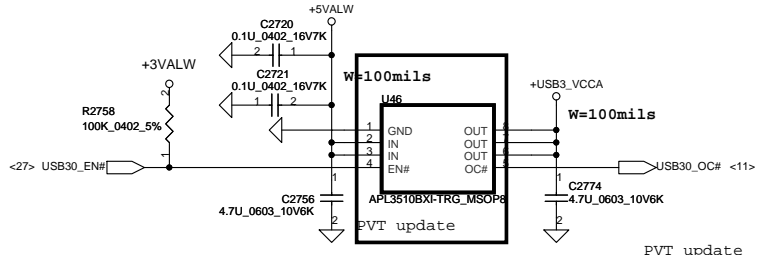
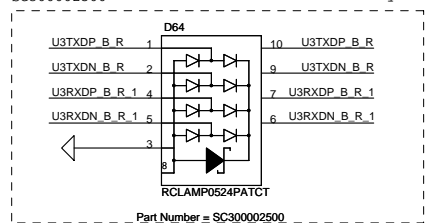
|   |                    |                 |            |     |
|---|--------------------|-----------------|------------|-----|
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| Compal Electronics, Inc.  |                    |                 |            | Rev |
| SCHEMATIC A9302   |                    |                 |            | Rev |
| 4019KC  |                    |                 |            | Rev |
| Date: Tuesday, October 30, 2012   |                    |                 |            | Rev |
| Sheet 25 of 41  |                    |                 |            | Rev |



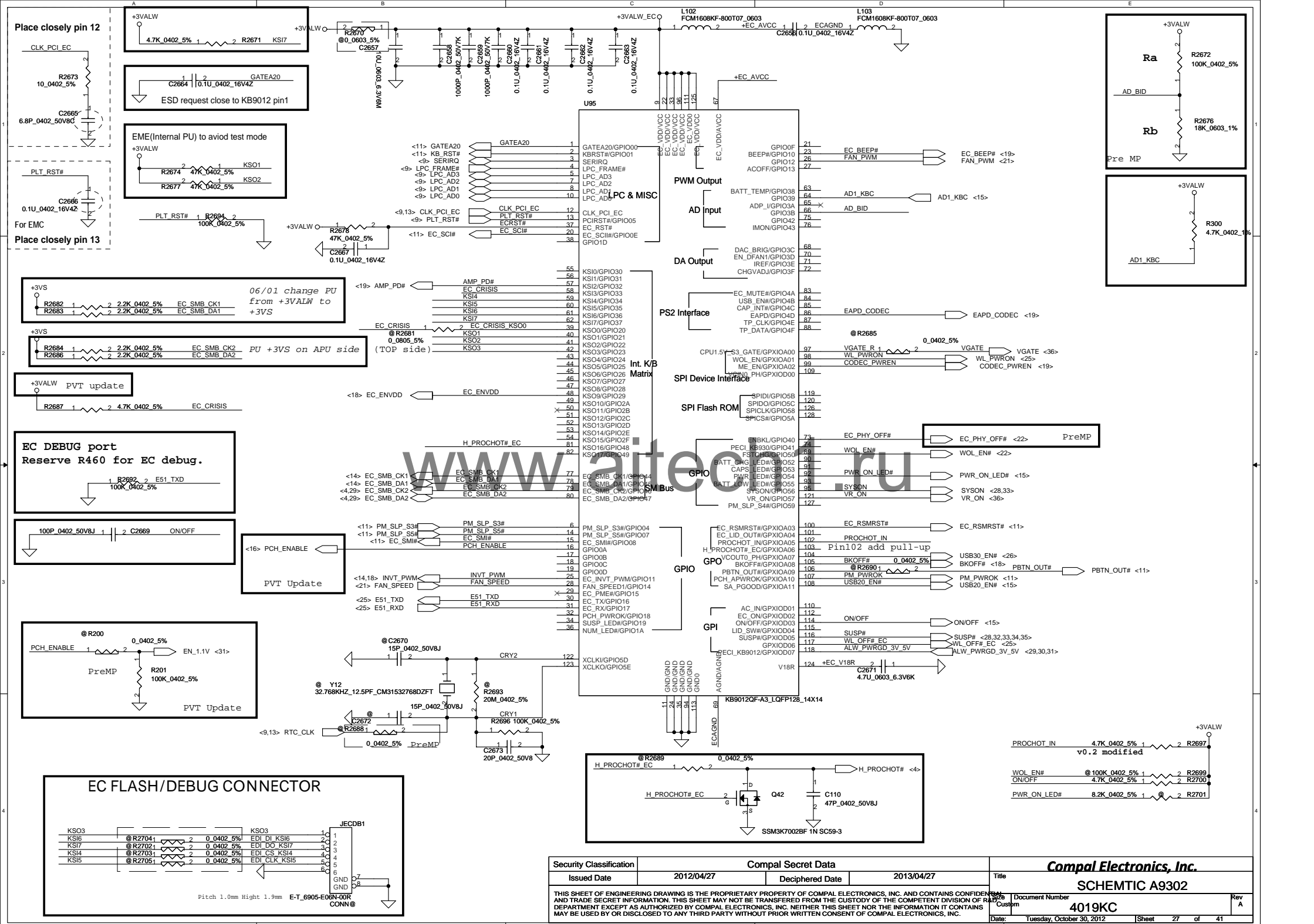
V0.4 : SC300000T10 change to SC300002500



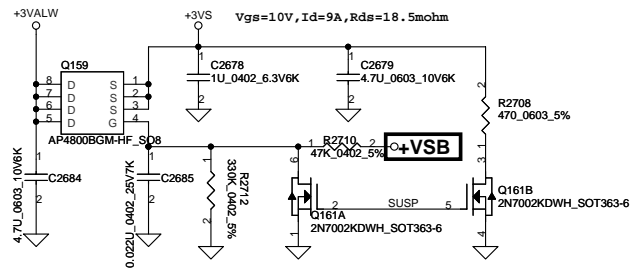
V0.4 : SC300000T10 change to SC300002500



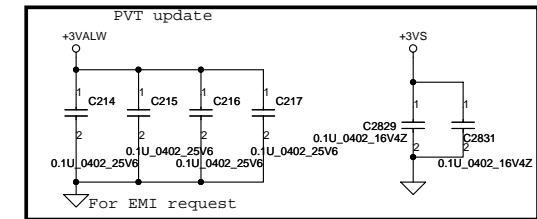
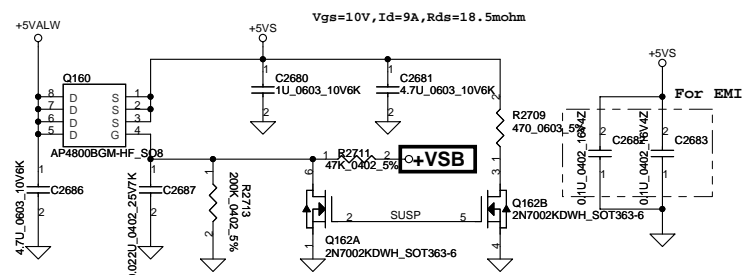
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|---|--|--------------------|--|---------------------------------|--|-----------------|--|
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|   |  |                    |  | Customer                        |  | A               |  |
|   |  |                    |  | Date:                           |  | Sheet 26 of 41  |  |



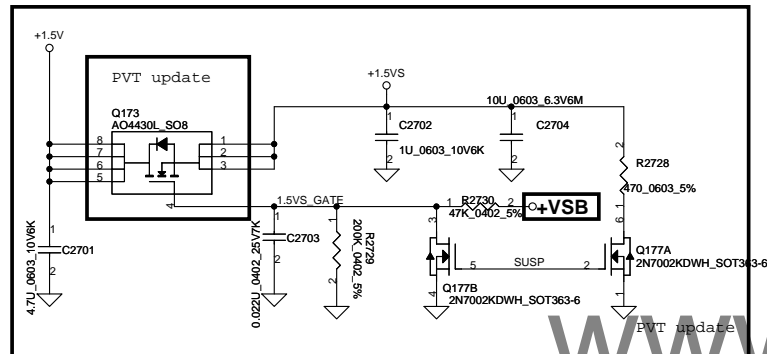
# +3VALW TO +3VS



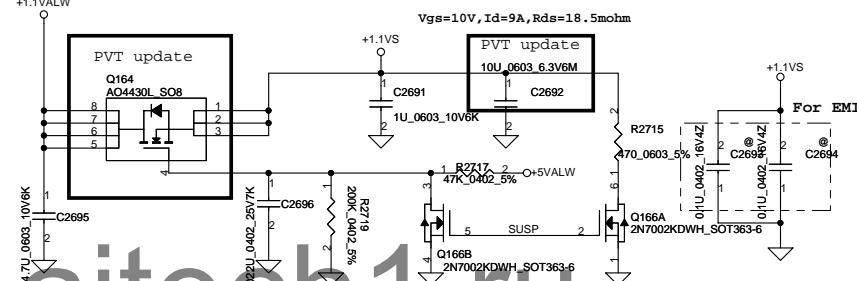
# +5VALW TO +5VS



# +1.5V to +1.5VS

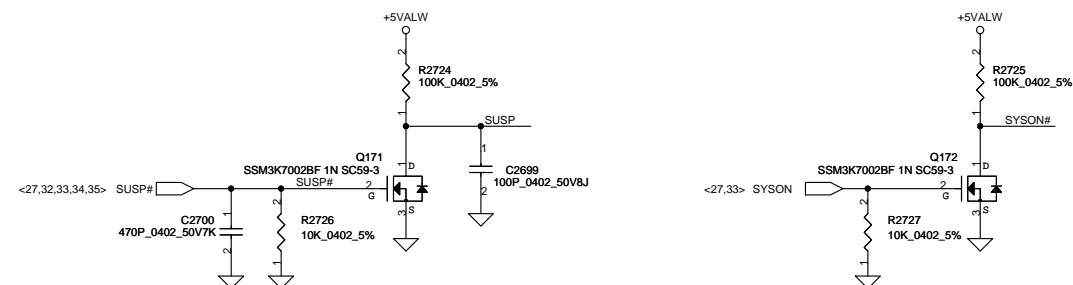
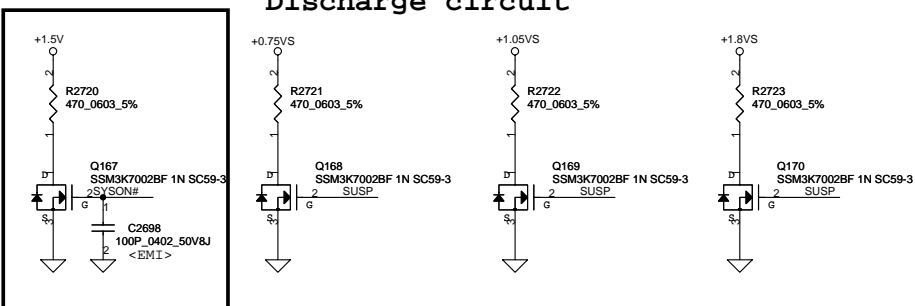


# +1.1VALW TO +1.1VS

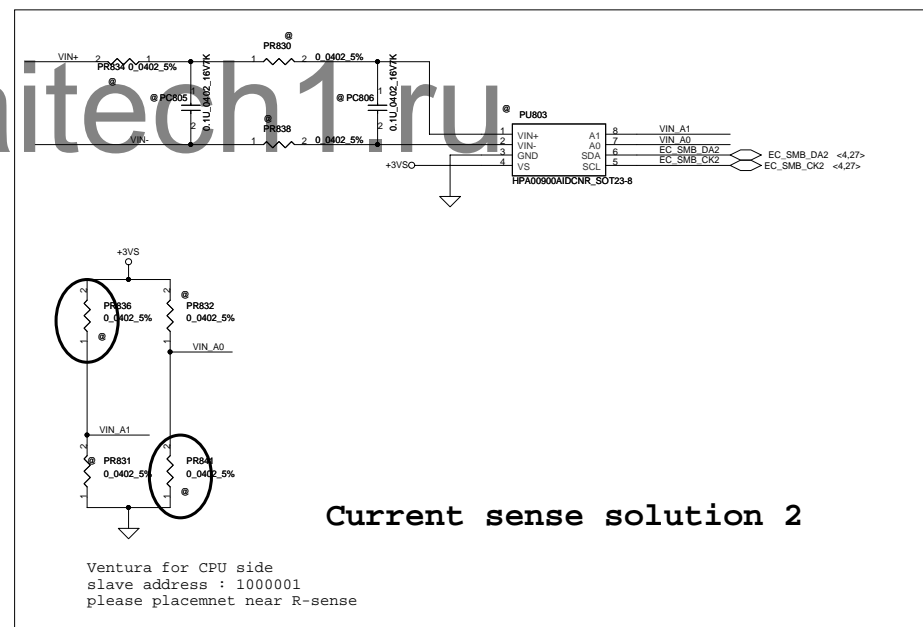
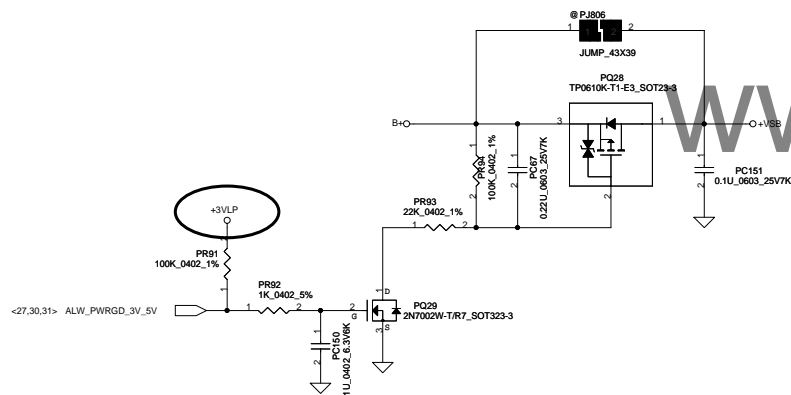
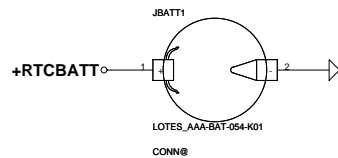
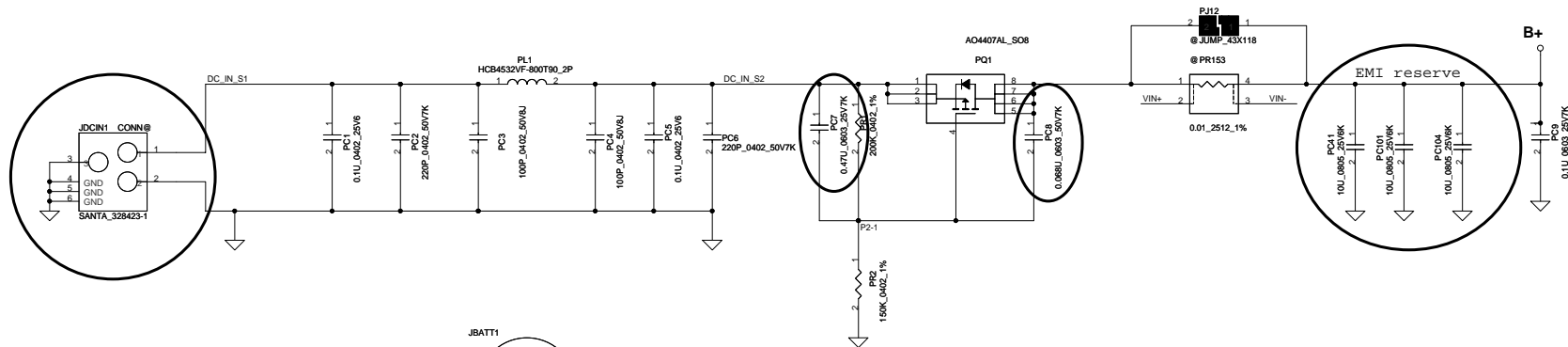


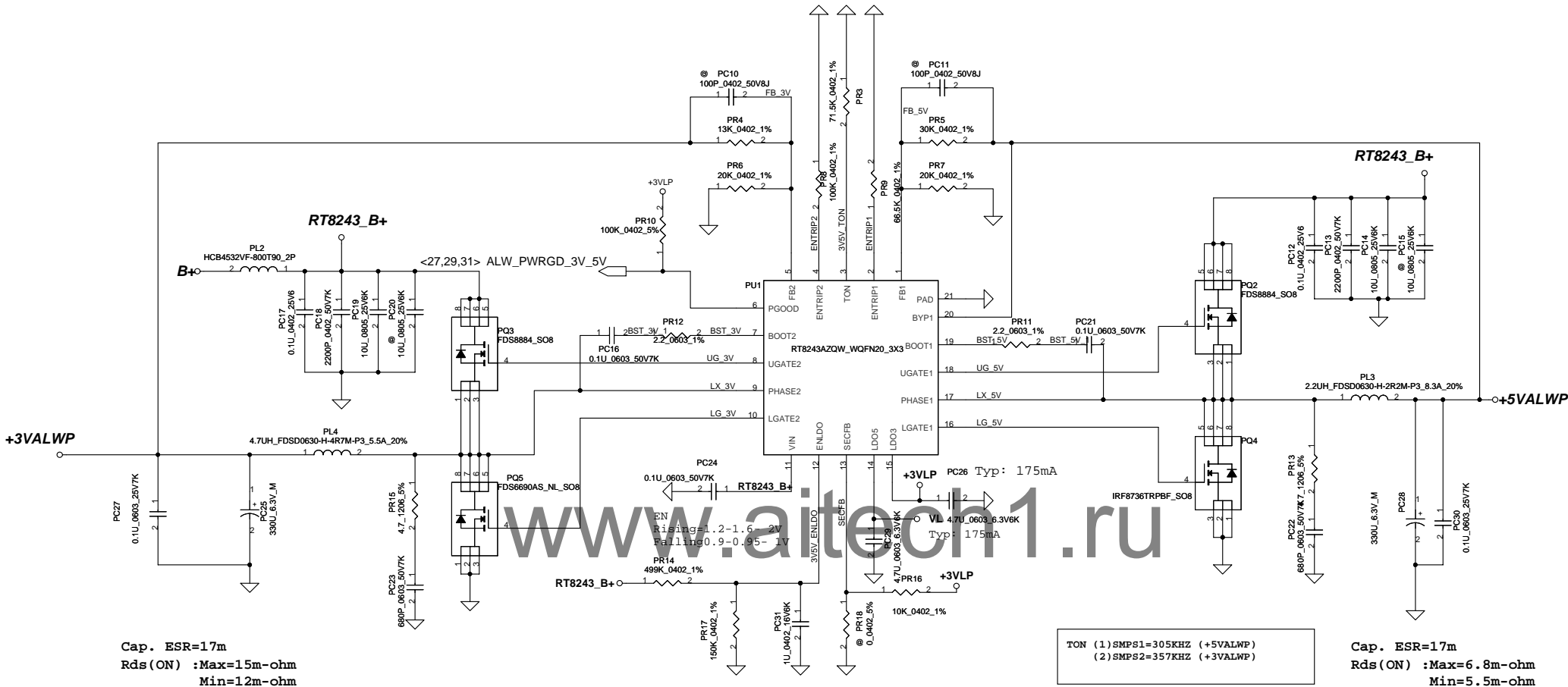
4/27 Add

# Discharge circuit



|   |                    |                 |            |                |
|---|--------------------|-----------------|------------|----------------|
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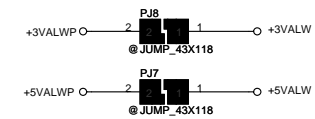


Cap. ESR=17m  
Rds(ON) :Max=15m-ohm  
Min=12m-ohm

+3VALWP  
Ipeak=5.44A ; 1.2Ipeak=6.52A; Imax=3.81A  
Fsw=357K,  
Iocp=6.6~8.417A

+5VALWP  
Ipeak=7.91A ; 1.2Ipeak=9.5A; Imax=5.98A  
Fsw=305K,  
Iocp=9.68~12.21A

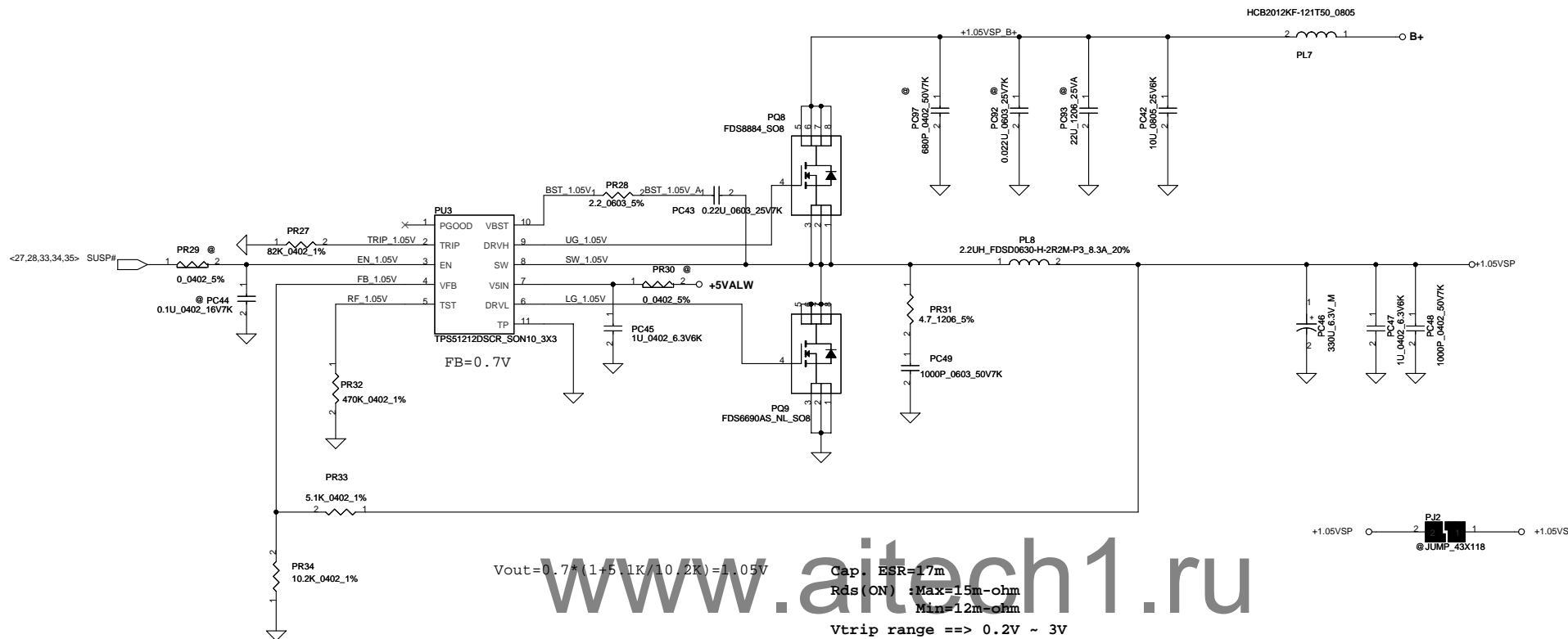
Cap. ESR=17m  
Rds(ON) :Max=6.8m-ohm  
Min=5.5m-ohm





$I_{ocp}(set) = 6.302 \sim 9.2A$

Date: Tuesday, October 30, 2012 Sheet 31 of 41



$$V_{out}=0.7*(1+5.1K/10.2K)=1.05V$$

Cap. ESR=17m

Rds(ON) :Max=15m-ohm

Min=12m-ohm

Vtrip range ==> 0.2V ~ 3V

<Vo=1.1V> VFB=0.7V

V=0.7\*(1+5.1K/10.2K)=1.05V

Fsw=290KHz

Delta IL=1.555A, Vripple=26.432mV

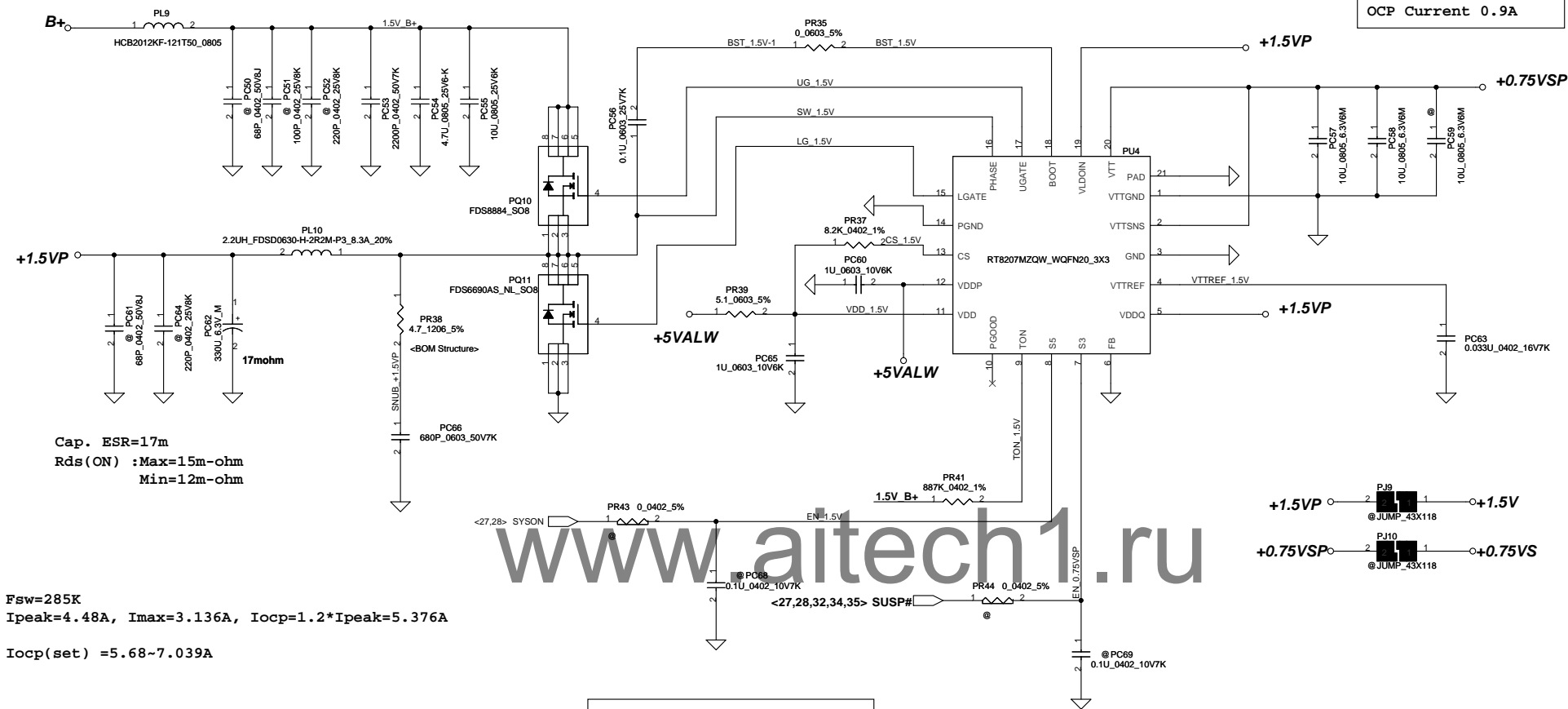
Ipeak=5.7A, Imax=3.99A, Iocp=1.2\*Ipeak=6.84A

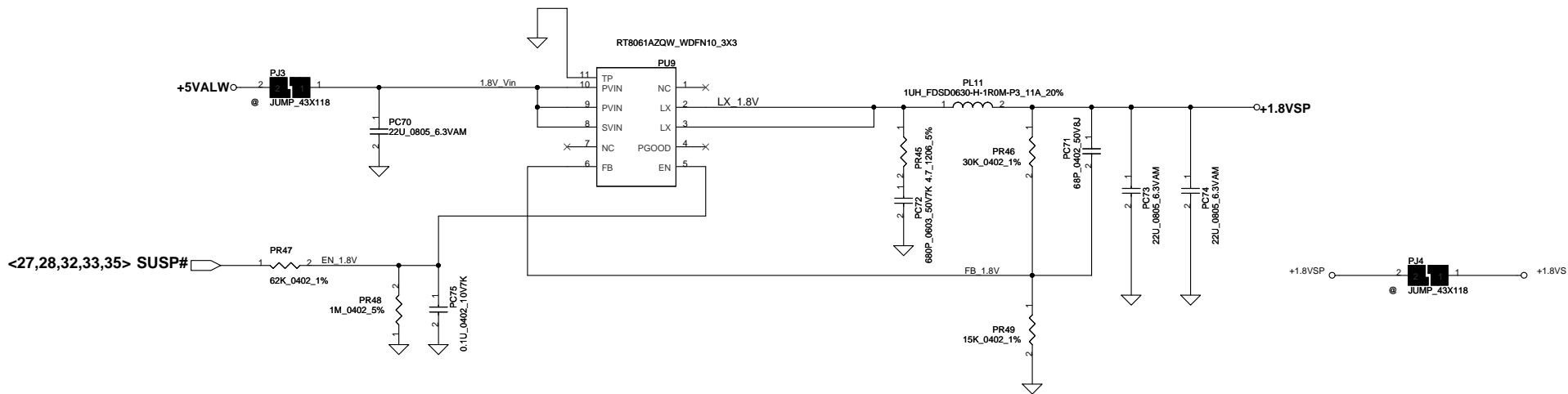
Iocp(set) =6.927~10.173A

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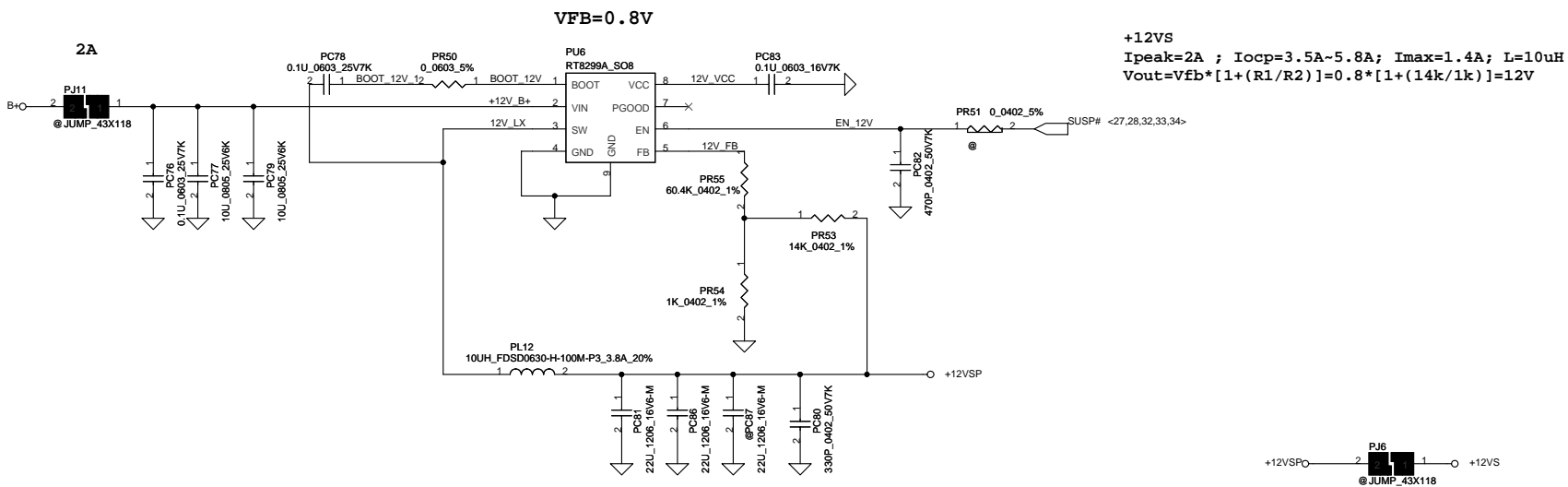






+1.8VSP  
 $I_{peak}=2.15A$  ;  $I_{max}=1.505A$  ;  $I_{oqp}=4A$  ;  $L=1\mu H$   
 $V_{out}=V_{fb} \cdot [1 + (R_1/R_2)] = 0.6 \cdot [1 + (30k/15k)] = 1.8V$

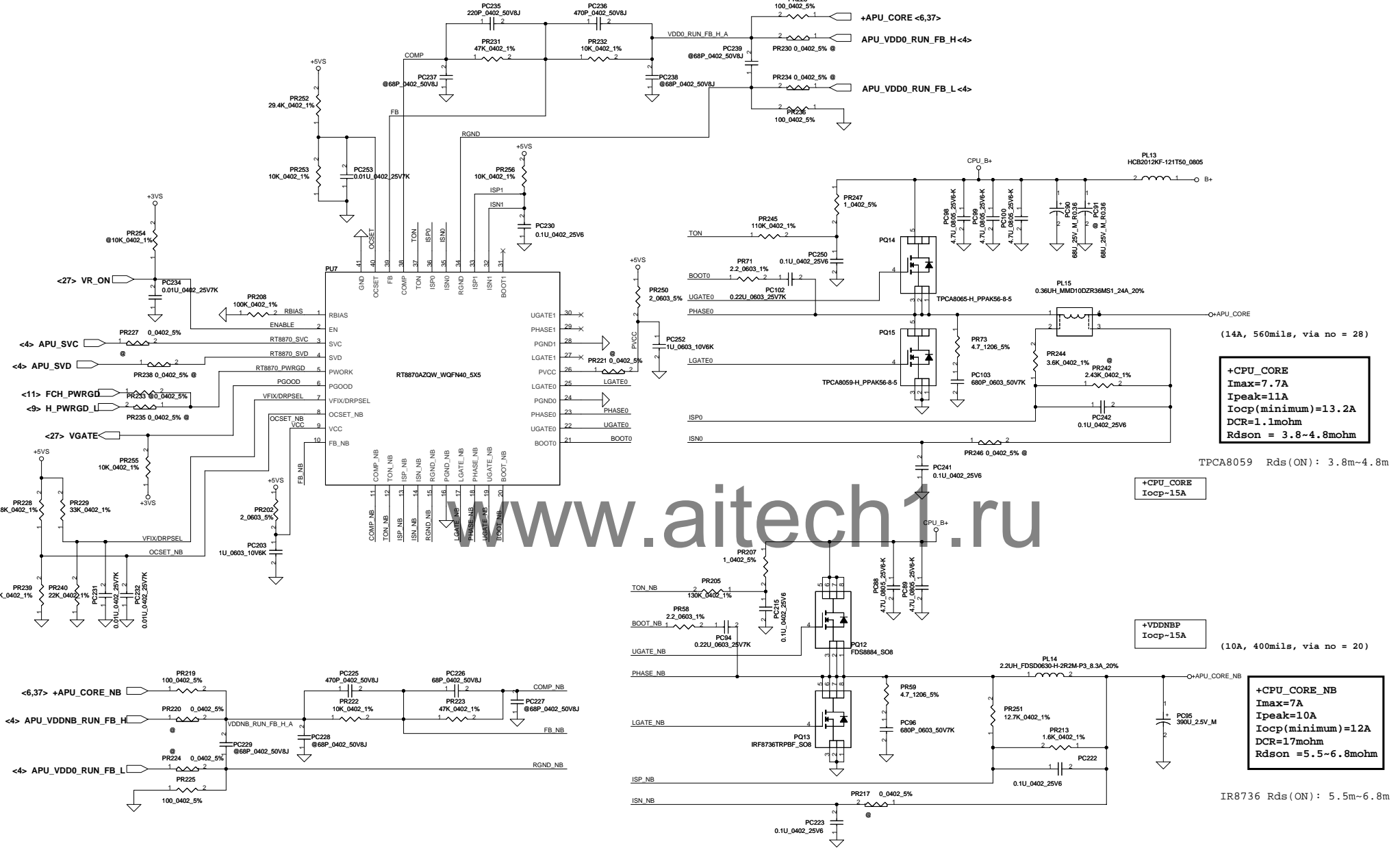
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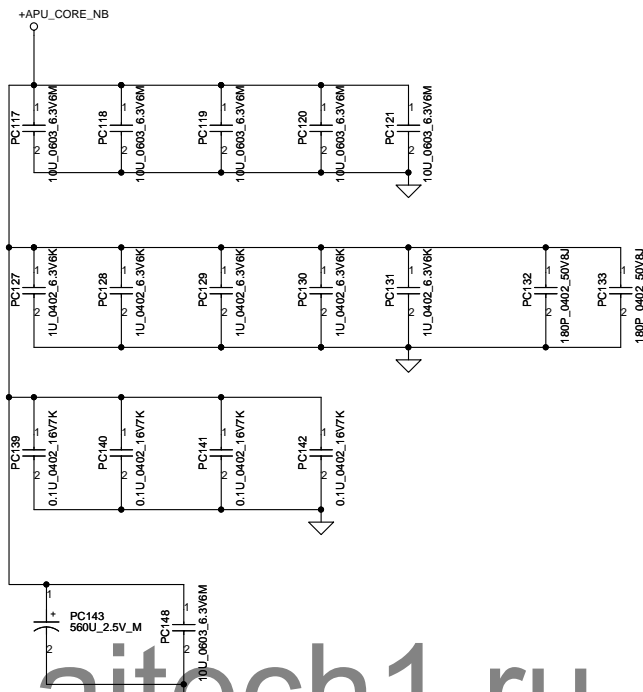
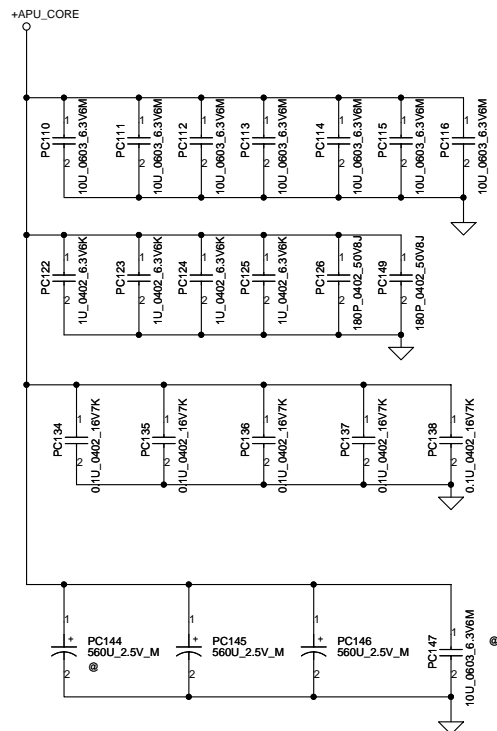
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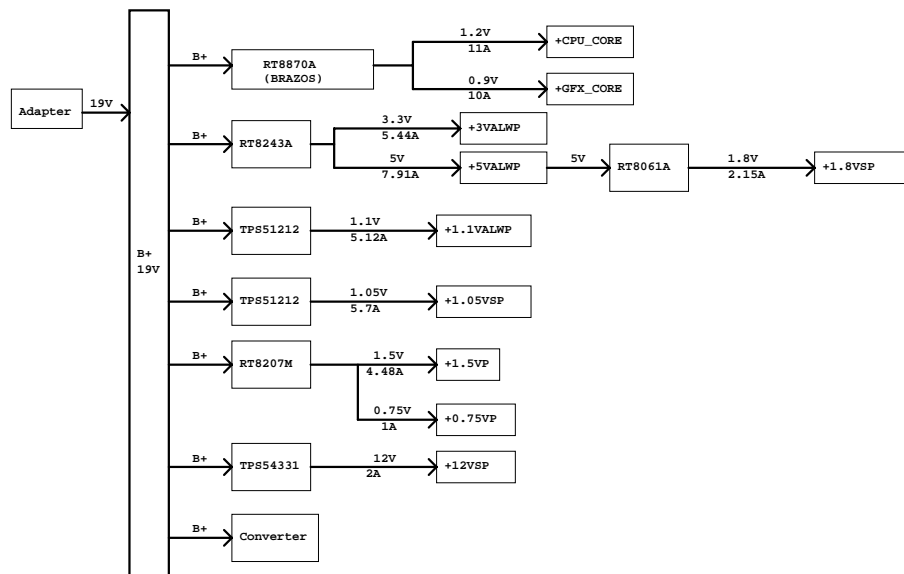


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Version Change List ( P. I. R. List ) for Power Circuit

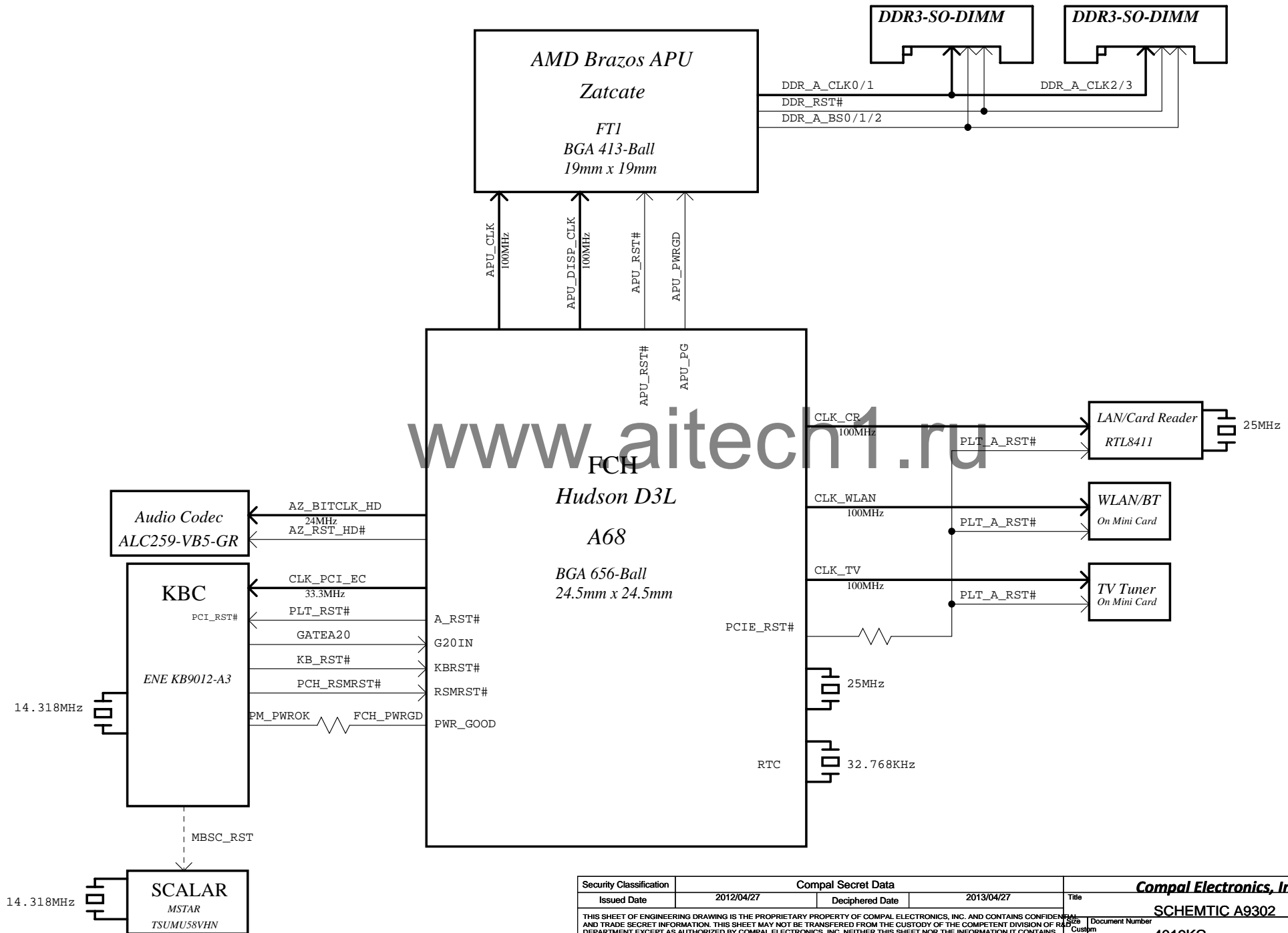
| DATE       | PAGE | COMMENTS  | Purpose                 |
|------------|------|---|-------------------------|
| 2012/05/30 | 30   | change PUI part number to SA00005VH00 (RT8243A)                         |                         |
| 2012/06/15 | 30   | change PR8=100K,PR9=66.5K   |                         |
|            | 33   | change PR37=8.2K  |                         |
| 2012/07/09 | 30   | change PR4=13K,PR6=20K  | Modify feedback voltage |
|            | 29   | change PC7=1UF  | for inrush current      |
|            | 36   | Remove BOM Structure "@ " of PR59,PC96                                  | CORE_NB MOS Snubber     |
|            | 35   | Change P35 12V circuit to RT8299A circuit                               | Design change           |
| 2012/07/13 | 36   | Remove BOM Structure "@ " of PR73,PC103                                 | V_CORE Snubber          |
|            | 29   | ALW_PWRGD_3V_5V Pull high with +3VLP                                    | for leak current        |
|            | 29   | change PC7=0.47UF   | for inrush current      |
|            | 31   | +1.1VALWP add Enable signal "EN_1.1V"<br>add BOM Structure "@ " of PR21 | HW request              |
| 2012/07/16 | 29   | change PC8=0.068UF  | for inrush current      |
| 2012/07/19 | 29   | change JDCIN1 and BOM Structure "CONN@"                                 | change DC-in Connector  |
|            | 31   | add PC84,PC85 and change PC32<br>and BOM Structure all "@"              | EMI request             |
|            | 32   | add PC92,PC93,PC97 and remove PC41<br>and BOM Structure all "@"         |                         |
|            | 33   | Remove BOM Structure "@ " of PR38,PC66                                  | 1.5V Snubber            |
| 2012/07/19 | 35   | change PR53 = 620K, PR54=44.2K  | modify Feedback res     |
| 2012/08/29 |      | change 0ohm res to short pad  | for cost                |
|            | 35   | change PR53 = 14K, PR54=1K,<br>add PR55=60.4K                           | modify Feedback res     |
| 2012/09/14 | 29   | Add PC41,PC101,PC104 = 10uF   | EMI request             |



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# Clock / Reset Diagram



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HW PIR (Product Improve Record)

- VBA10 Change List(EVT --> PVT)
- 1. change R2786-2 from U98-18 to U98-13
  - 2. change R2786 from 5.1K to 39.2K
  - 3. change U98-31/30 to MIC\_VREF0\_L/R
  - 4. R2777-1/R2776-1 change to connect MIC\_VREF0\_L/R
  - 5. change D68/D69 location. D68-2 to PD#. D69-2 to U98-4
  - 6. change c2678 from 10u to 1uF\_0603 modify JRJ1 to UDE-RV-27225NBA
  - 7. U99-51/49/43 add LAN LED signals
  - 8. change R2490 to @, R2491 change to POP
  - 9. R501 change from default short to 0\_ohm
  - 10. JFAN1 change to ACES 85204-04001 and location
  - 11. JSPK1 change to ACES 85204-04001 and location
  - 12. JLED change to ET-6905\_E06N\_00R ,6 pin and location
  - 13. EC\_CRISIS change PU to +3VALW
  - 14. Q163 (1.1VALW) change from AP4800 to AO4430L
  - 15. C2692 change from 4.7uF to 10uF\_0603
  - 16. Del JHDT1,R2505,R2506,R2499,R2500,R2503
  - 17. Add C210,C211,C212 (0.1uF) on +3VS,C213 on +3VALW for EMI request
  - 18. Change LAN IC clk from GPP\_CLK0P/N to GPP\_CLK5P/N
  - 19. Change R77-R86 from default short to 0\_ohm (PCIE clk
  - 20. Change R2783 from 0.1uF\_0402 to 1uF\_0603
  - 21. EC pin16 add PCH\_ENABLE to control +3VALW\_FCH and +1.1VALW
  - 22. Add +3VALW\_FCH ckt (C562,C564,C563,C1862,Q88,Q177,Q119,R1762,R1763,R1764,R1765)
  - 23. Add C2560 on DDR\_RESET# for EMI request
  - 24. Page10~13, change FCH 3V power from +3VALW to +3VALW\_FCH
  - 25. Delete H8 H23, Add JP1 JP2 for FCH Thermal
  - 26. U46, U96 change from SA000039E00 to SA00003DR00
  - 27. New circuit for +1.5V to +1.5VS, Add damping R on Y1,Y13
  - 28. add R1803 (0\_0603) for +5VS and +HDMIOUT\_EDID\_5V\_F
  - 29. Add R2798-R2801 on JSPK1 for EMI Request
  - 30. Add L177 L178 C218 C219 on JLED1 +3VS +3VALW for EMI Request
  - 31. Add C2829 C2831 for EMI request
- PVT --> PreMP
- 32. EMI request C2491 C2496-C2499 C2500 C2501 C2514-C2516
  - 33. Unpop C126 C127
  - 34. Add Short pad to replace the 0ohm
  - 35. Unpop U101 and relevant parts and Pop the R2856
  - 36. Add L192 ~ L195 , C2773 C2775 C2776 C2778 for EMI request
  - 37. EC Pin73 (EC\_PHY\_OFF#) Connect to GPO
  - 38. Add 10ohm and 5pF on SD\_CLK for EMI request
  - 39. JRJ1 LED Power Connect to +LAN\_VDD\_3V3
  - 40. Unpop all TV fuction.
  - 41. Delete D10 D11 add D76 D77 for EMI request.
  - 42. Update the BIOS U93 Symbol.
  - 43. Update the JODD1 JHDD1 JODP1 JHDP1 symbol and Footprint

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